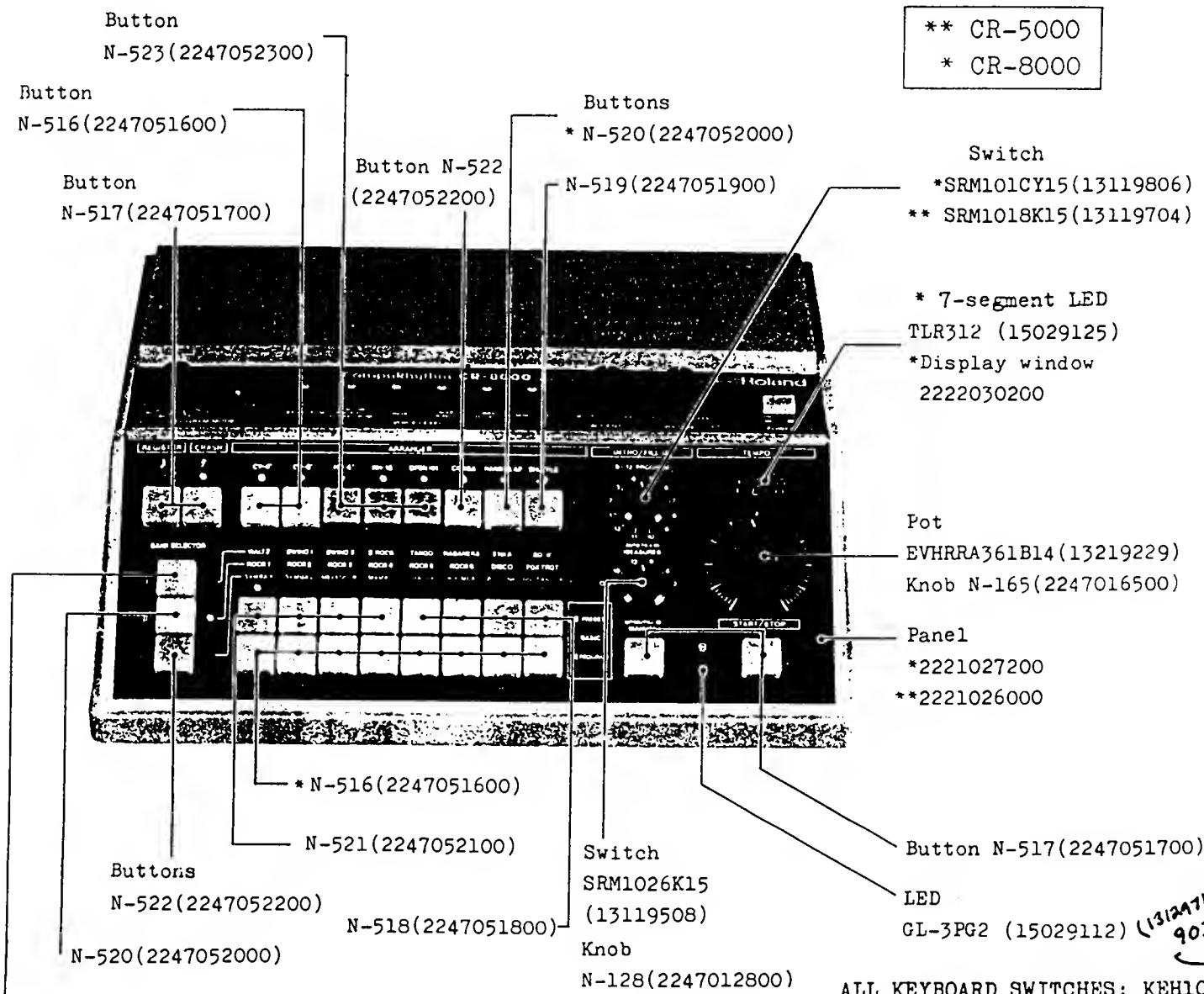


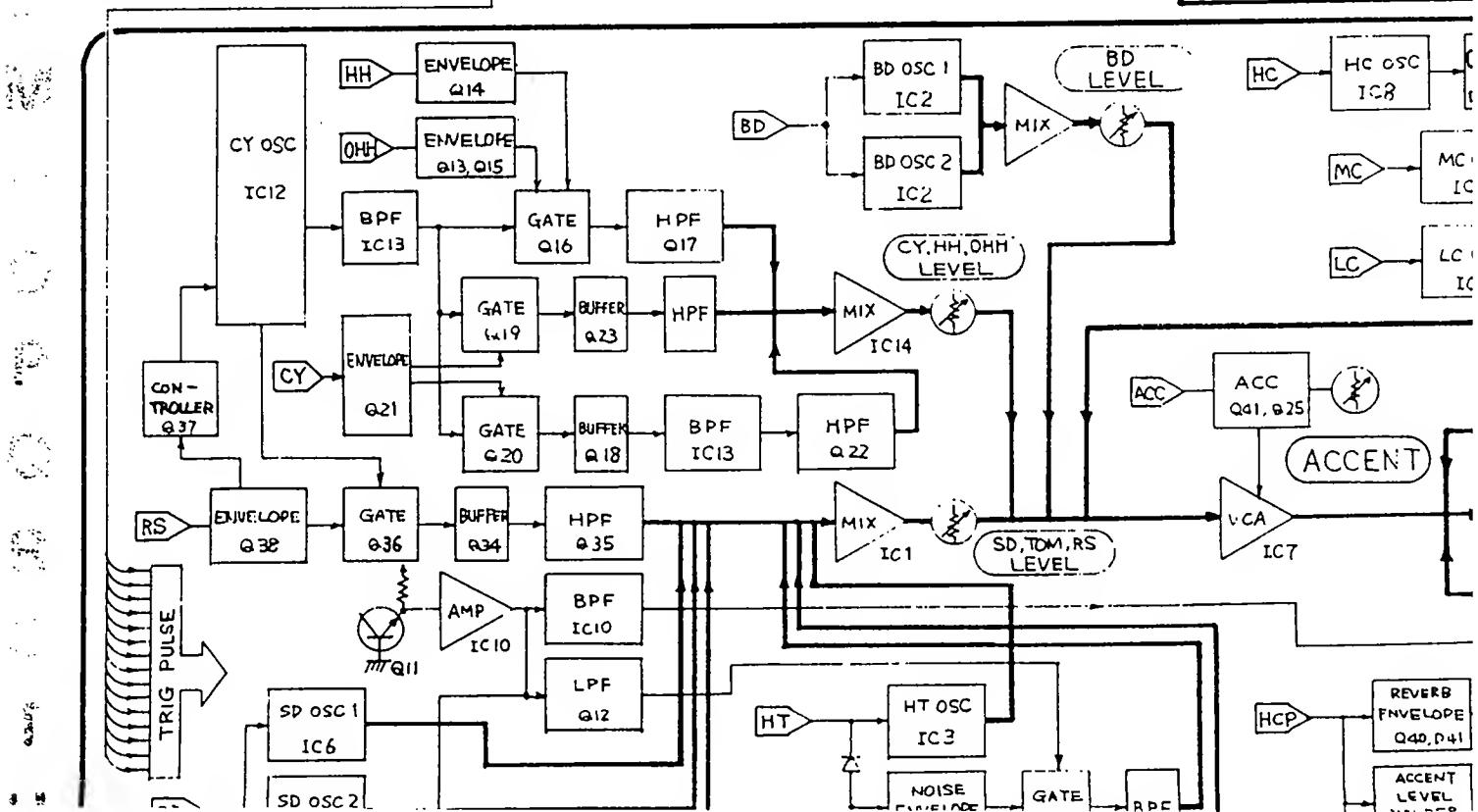
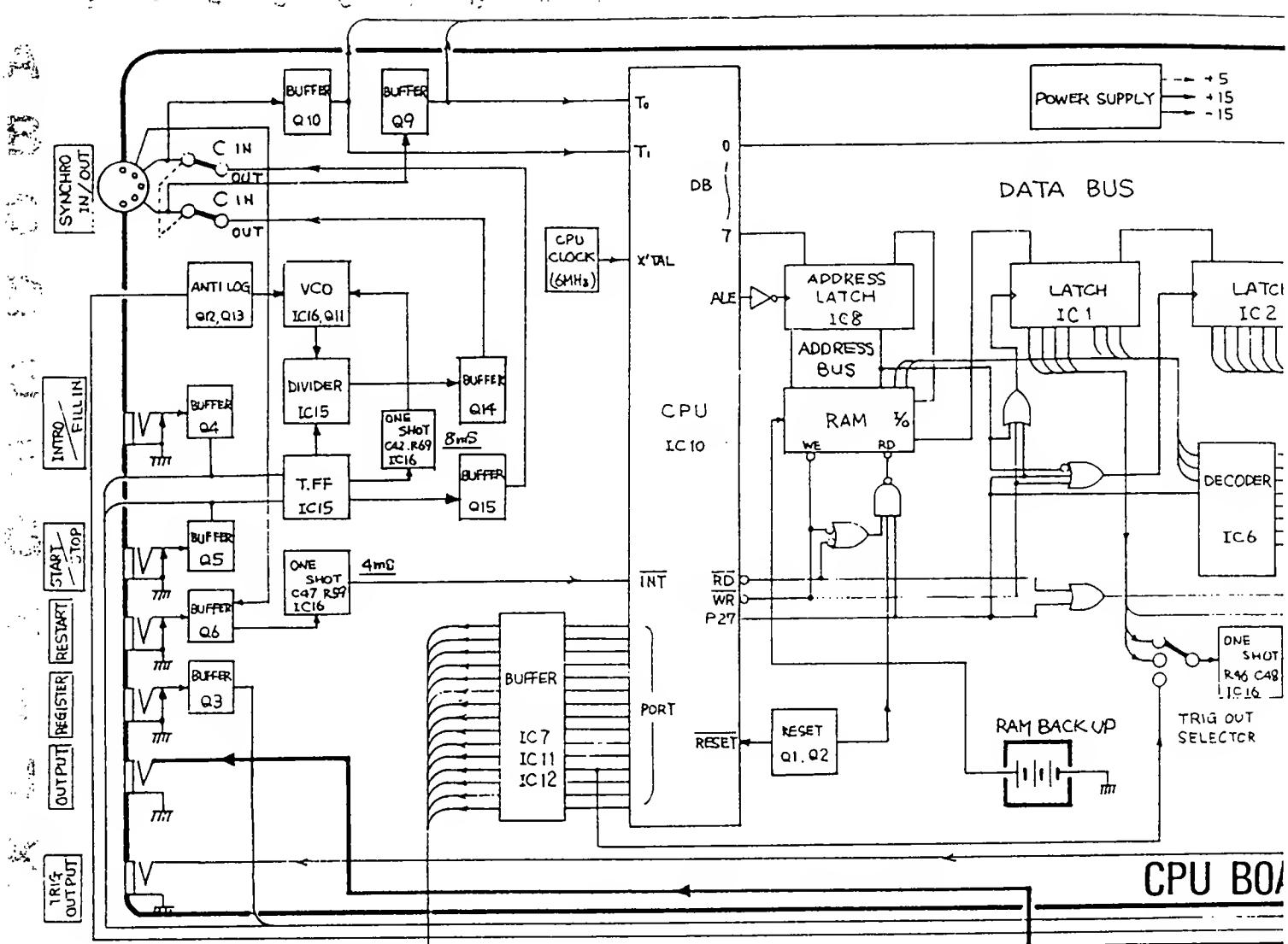
**CR-5000/8000 SERVICE NOTES****SPECIFICATIONS***First Edition*

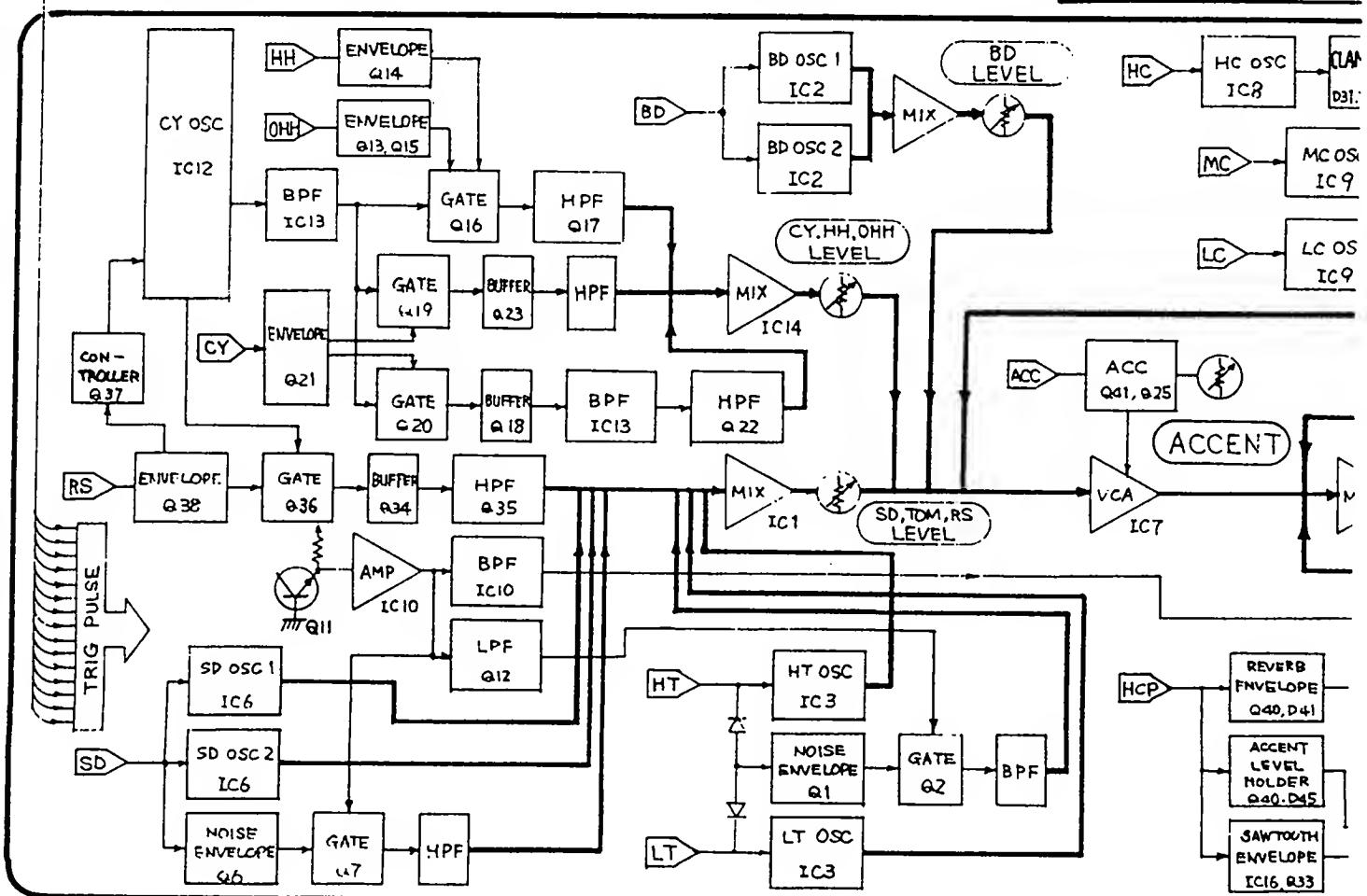
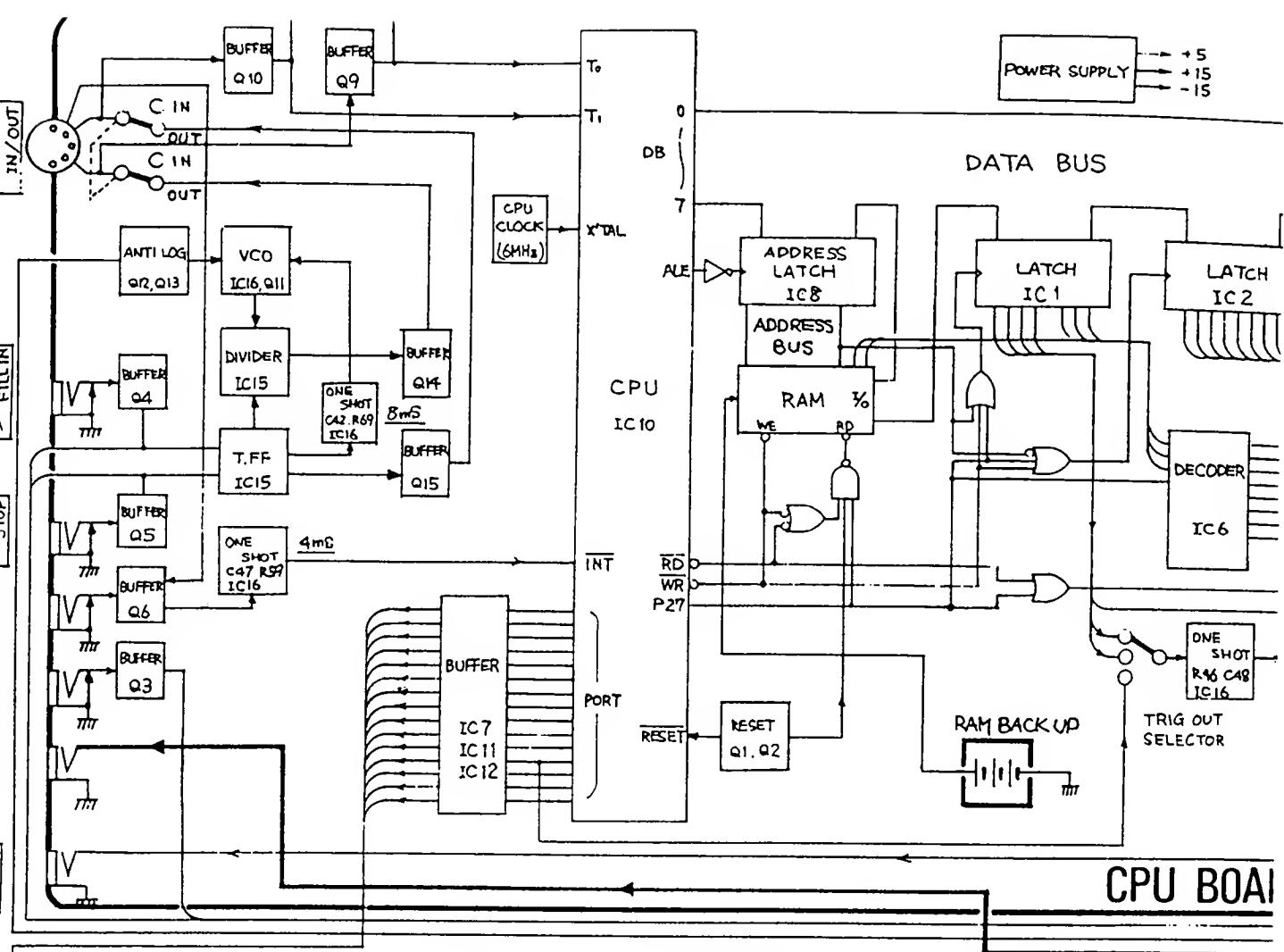
Second Printing (July 12, 1983 E2)

OUTPUT IMPEDANCE .... Less than 6KΩ or less than 25KΩ (Serial No. CR5000 091100-, CR8000 090900-)  
 TRIGGER OUT .... Level: +5 positive edge  
 Width: 44ms (typ) @ TEMPO min./12ms (typ) @ TEMPO max.  
 OUTPUT (max.) .... 4V p-p @ VOICE LEVEL max./VOLUME max./ACCENT min. (16V p-p @ ACCENT max.)  
 (into 100KΩ) 2.5V p-p @ VOICE LEVEL mid./VOLUME mid./ACCENT mid.  
 (CR8000)  
 SYNC IN .... +15V (max.)  
 SYNC OUT .... +15V (Tempo clock - 6.7ms-71ms)  
 POWER CONSUMPTION .... CR5000: 10W, CR8000: 12W  
 DIMENSIONS .... 331(W) x 278(D) x 108(H)mm  
 WEIGHT .... 3.7kg  
 NOISE .... 0.3mV rms (-68dB) (0dB = 0.775V)  
 (load 100kΩ) (DIN 45405 wtd)



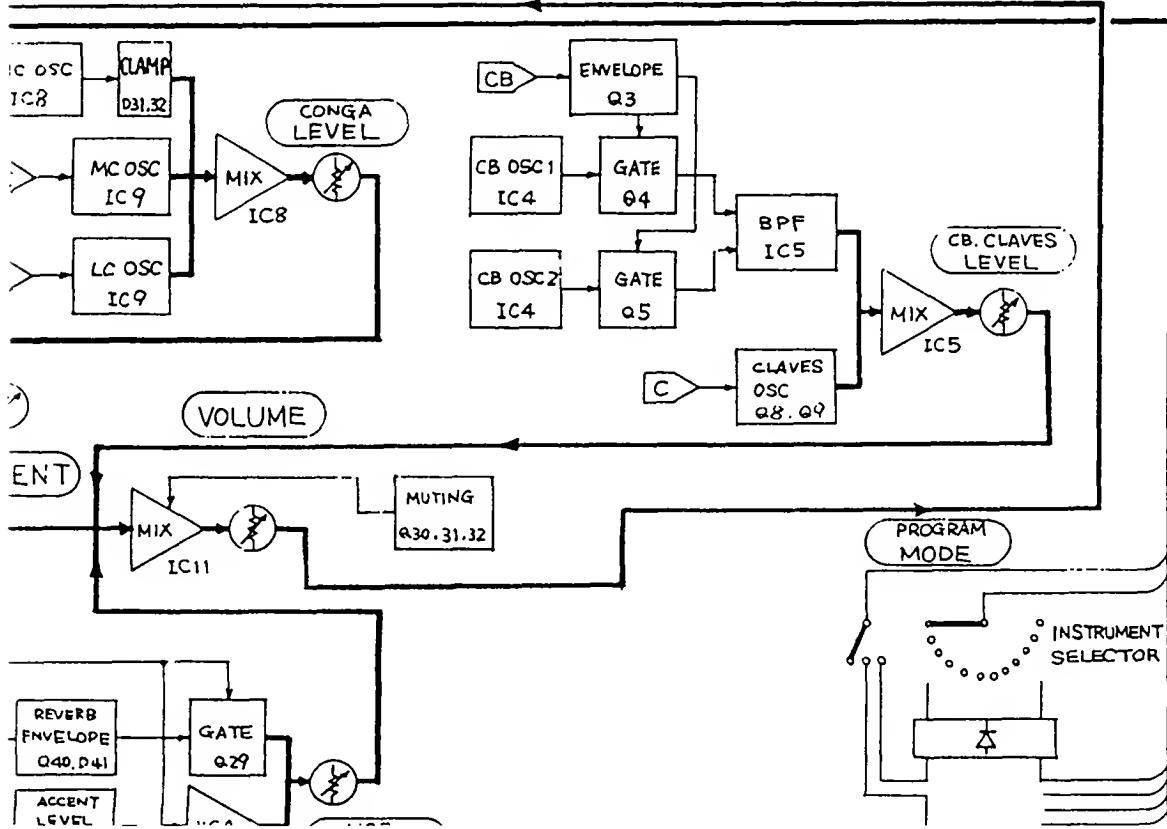
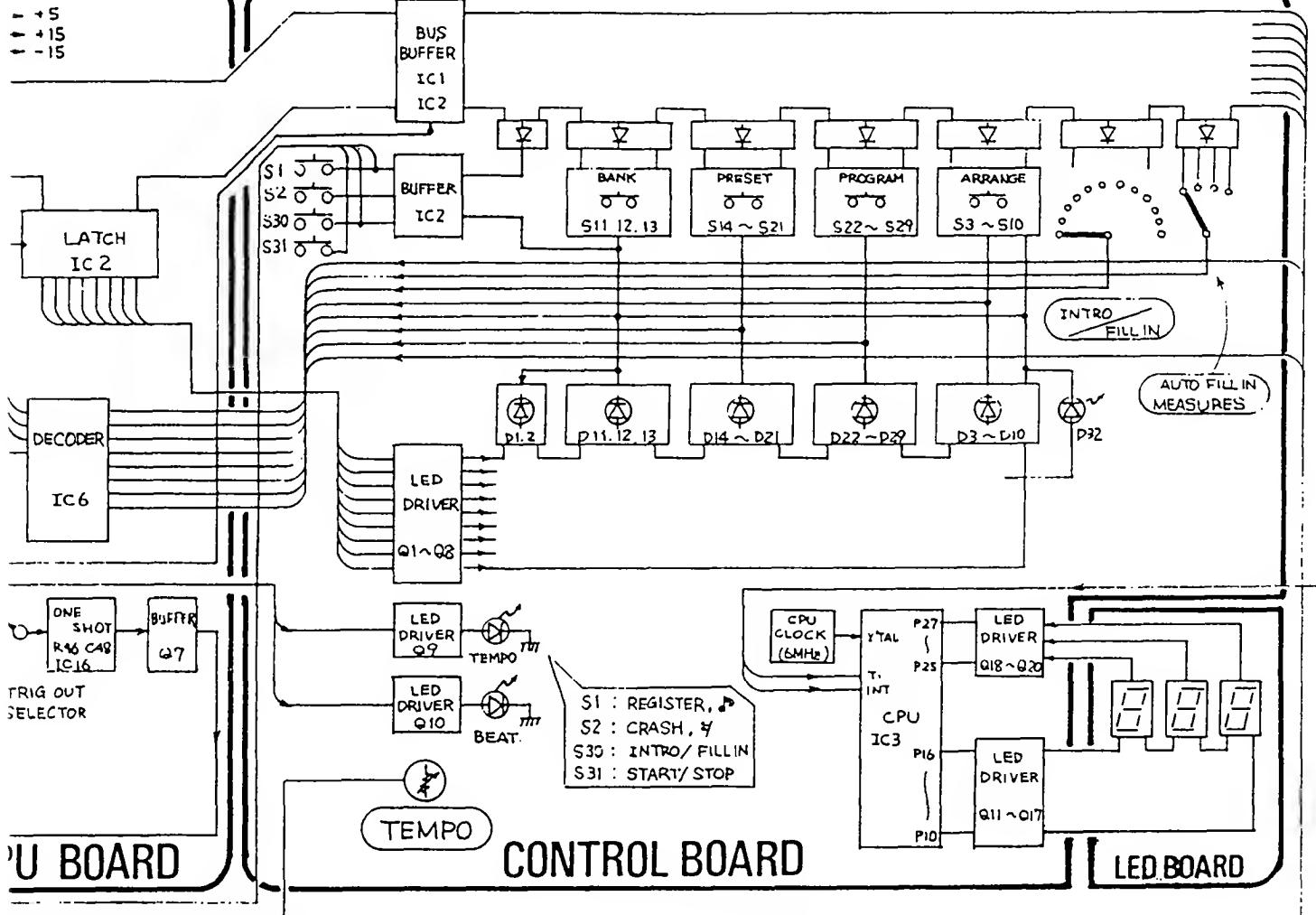
# CR-5000/8000



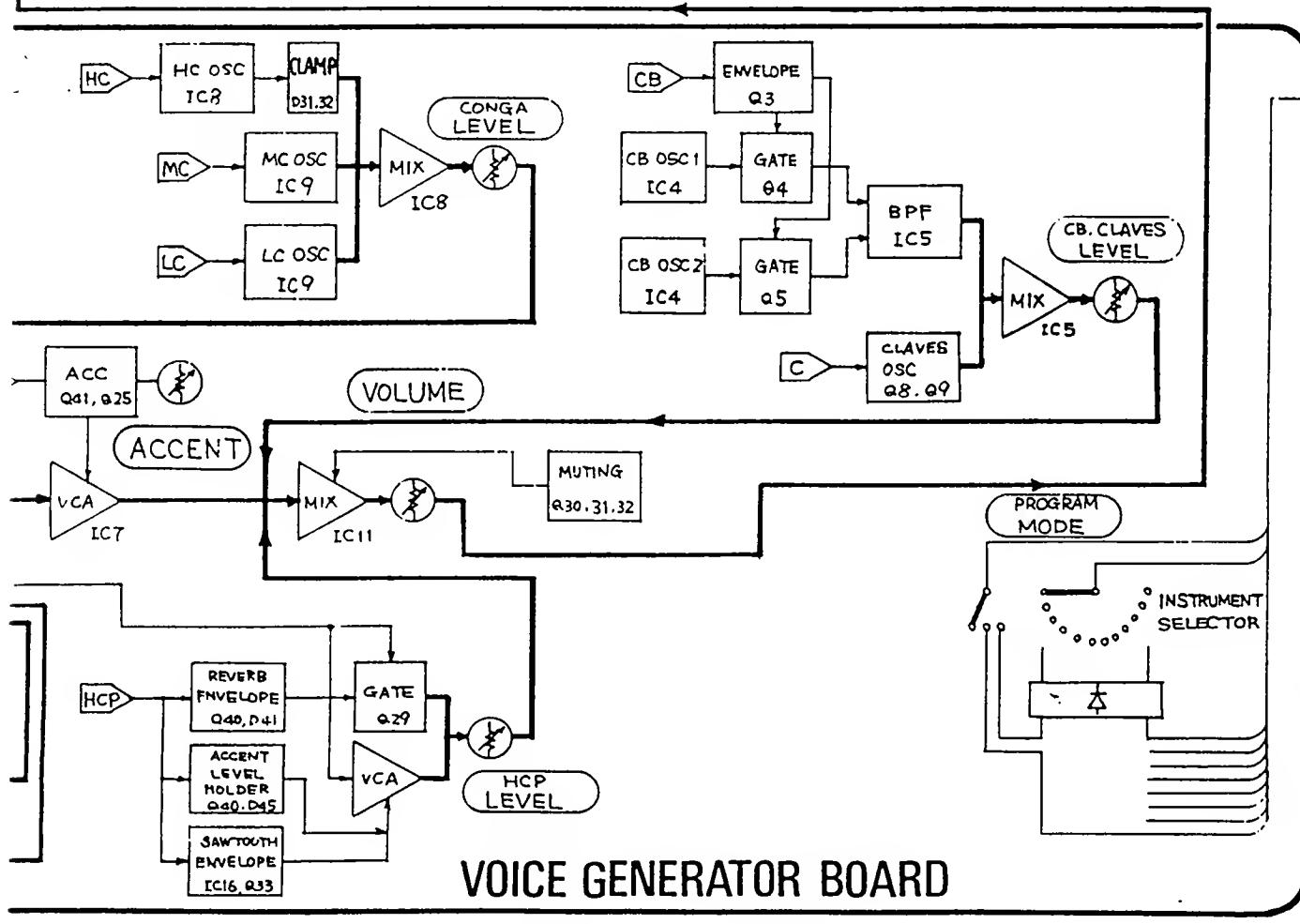
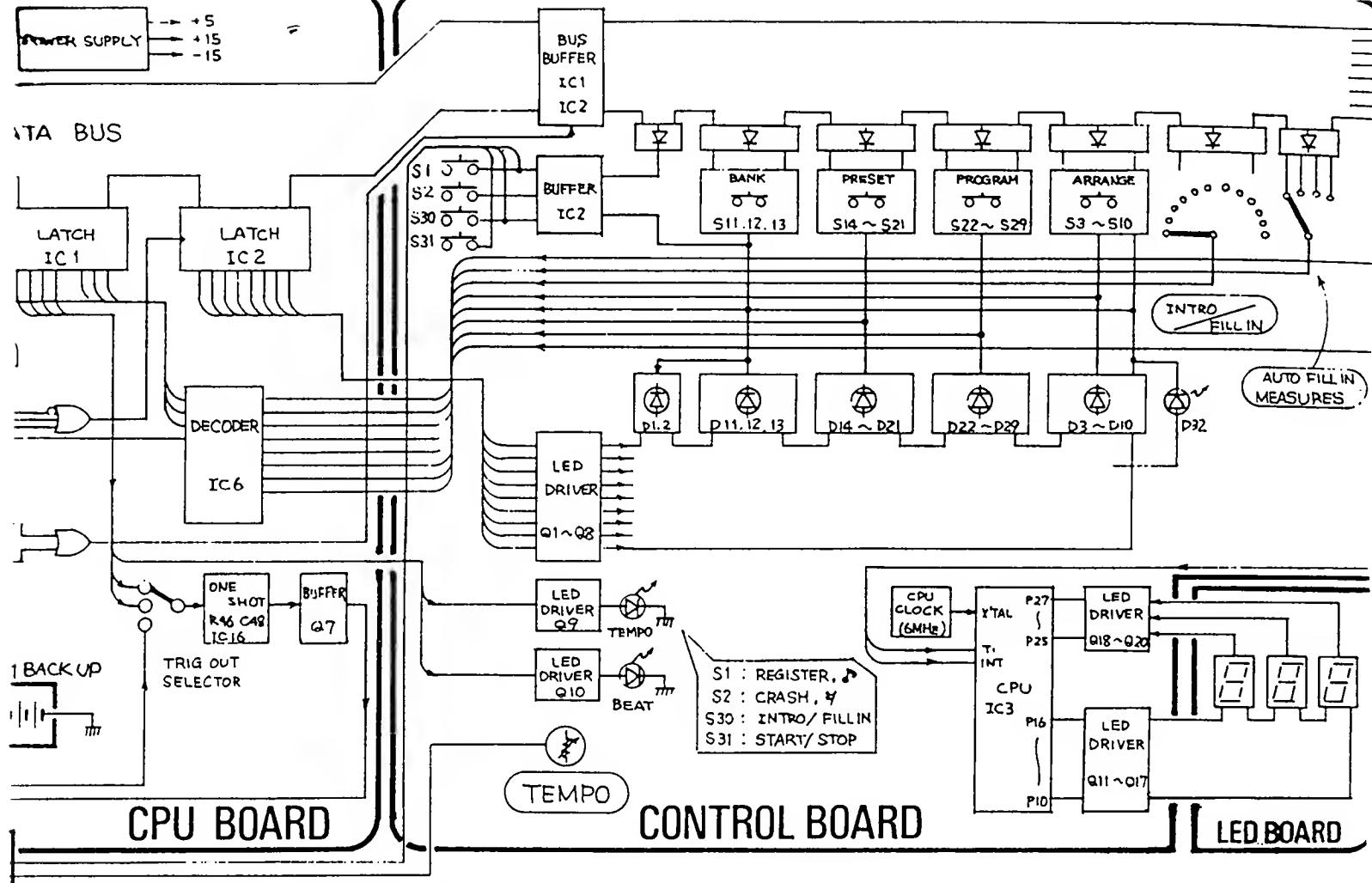


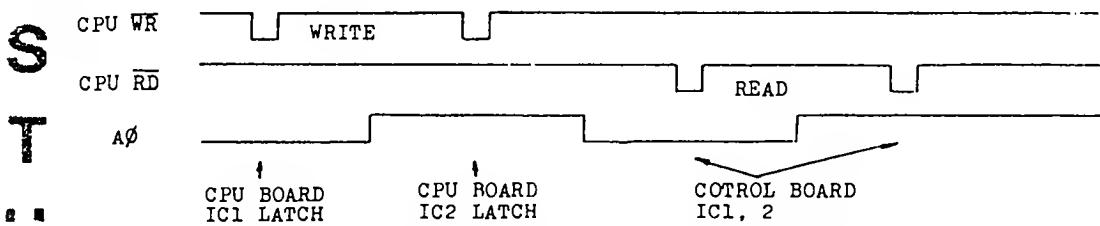
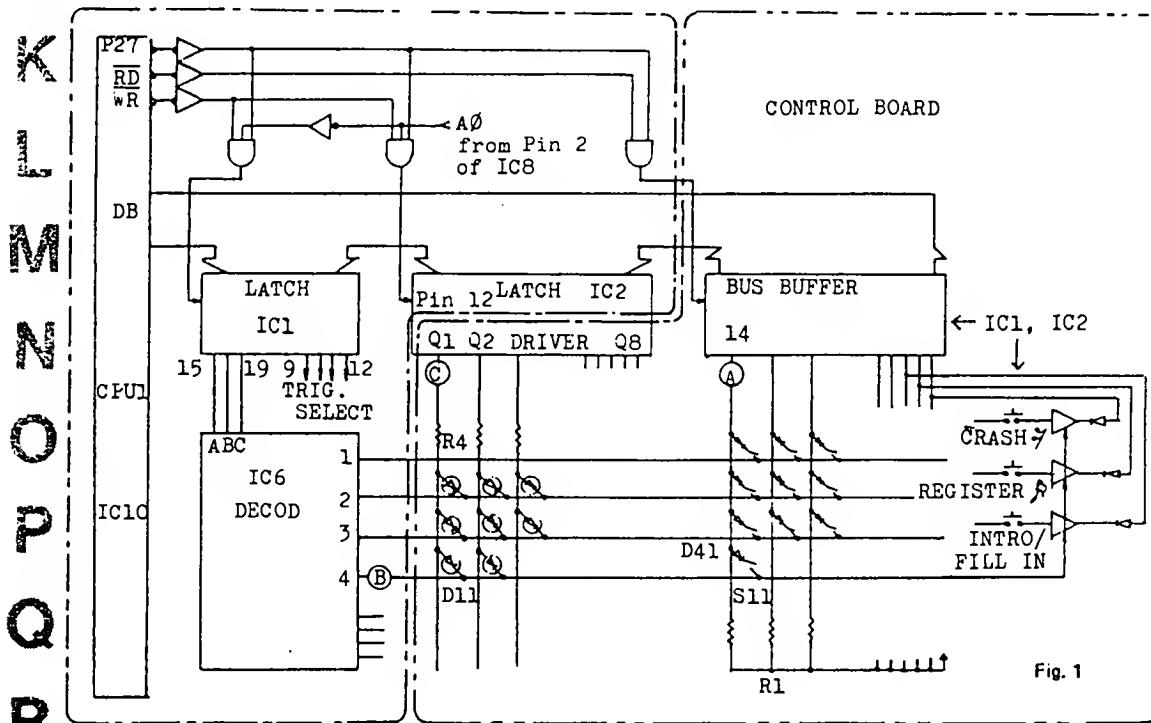
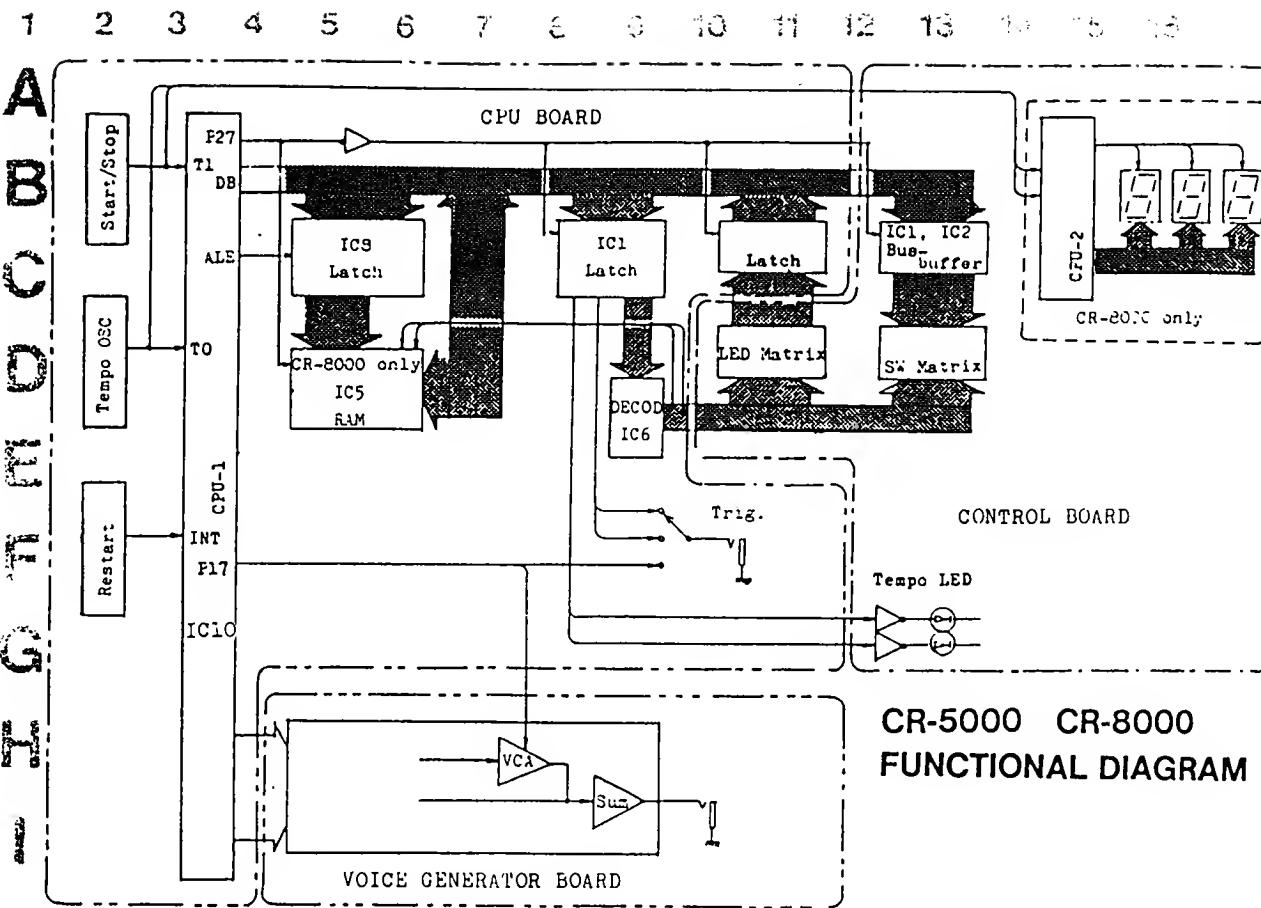
DEC.8, 1981

19 20 21 22 23 24 25 26 27 28 29 30 31



CR-8000  
BLOCK  
DIAGRAM





18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

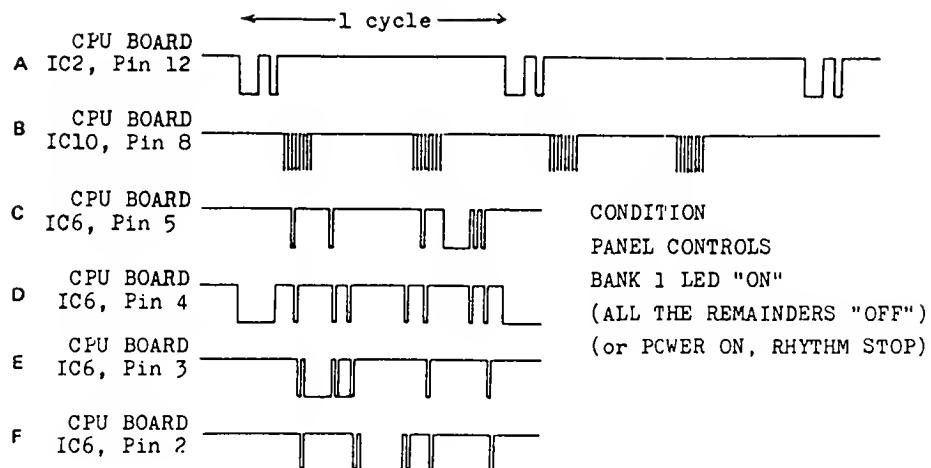


Fig. 2

## CIRCUIT DESCRIPTION

### SWITCH SCANNING

CPU holds one of switch matrix rows low through LATCH IC1 and DECODER IC6.

Ex. When S11 closes while pin 4 of IC6 (B in Fig. 1) is held low, pin 14 of BUFFER IC1 (A in Fig. 1) which is pulled up via R1, becomes low. This low is read by CPU through data bus.

CPU continues this sequence for the remaining 7 matrix rows (B, Fig. 2).

Once rhythm starts, time interval between switch scanning varies to Tempo Clock rate.

### LED DINAMIC SCANNING

To light LED that is on, CPU selects matrix row and column where the LED is connected diagonally.

In the above example D11 has been on, CPU fires LED driver Q1 through LATCH IC2 in sympathy with low at B in Fig. 1 (A and D in Fig. 2.)

Lengths of lows and intervals between lows in Fig. 2 also vary greatly with controls setting and rhythm tempo.

### VOICE TRIGGER SIGNAL

CPU delivers trigger signals (negative going) to individual VOICE Generators.

Trigger signal goes negative at the falling edge of tempo clock and stays low until the next falling edge of the tempo clock. That is, width of trigger signal is equal to period of one clock signal. The maximum trigger signal rate is  $\frac{24 \text{ clocks}}{4}$  (B).

**EXT TRIGGER** Derived from LATCH IC1 on CPU board. They are also negative going and the pulse width is equal to that of tempo clock.

### RESTART

CPU reads INT terminal (not in use for interrupt application) every 3ms and, when INT is high, resets internal counter to revert to onset of a measure.

If monostable (1/6IC6, C47 and R59) output is high for a period shorter than 3ms or

## GE GENERATORS

the voice generators are designed based on a fashion similar to those detailed in the circuit description the TR-808 Service Notes which is expected to be referenced to as necessary. Exceptions are Cymbal and Shot. Below brief comments on individual voices.

circuit consists of two bridged-T networks.

↳ has two bridged-T filters for drum sound, in addition, noise generator for snare sound.

11

laged-T networks in these stage include two diodes in their RC constant loop. The diode changes con-  
ting rate in proportion to sound amplitude passing  
ough the network, changing filter characteristic,  
shifts filter response curve (frequency) along  
d contour. Pink noise is combined with this out-  
to simulate reverberation.

1C. HC

↳ based on Bridged-T. HC output is clamped on D31-D32 to have multiple harmonics to emphasize highs.

2000-01

combined square waves from Shmitt triggers are gated at choppers with the contour set by respective envelop generator outputs.

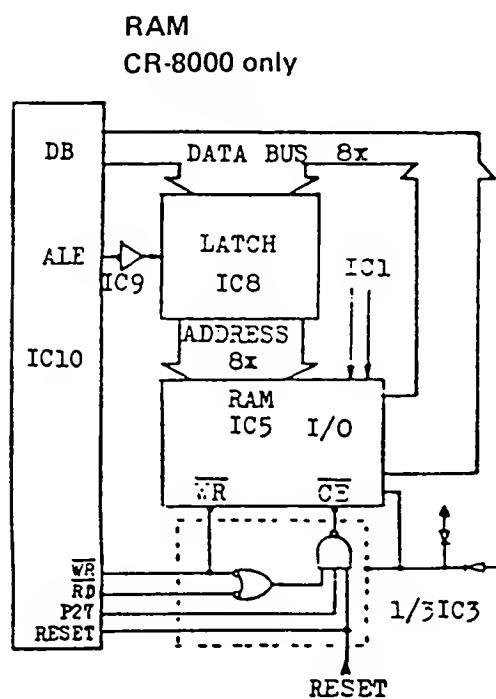
ng six Schmitt triggers, two are used which reset by an RS trig fed through Q37. The first rising edge of two outputs are synchronized to each other to eliminate unsavory sounds the very first of RS note.

CB

Two oscillator outputs of frequency are summed at B: gated at choppers.

HCP

HCP sound is accomplished  
lating white noise with sa  
waves derived from TC6



## NOTES:

P27 - high during RAM accessin,  
CE - high during power off

## ACCENT

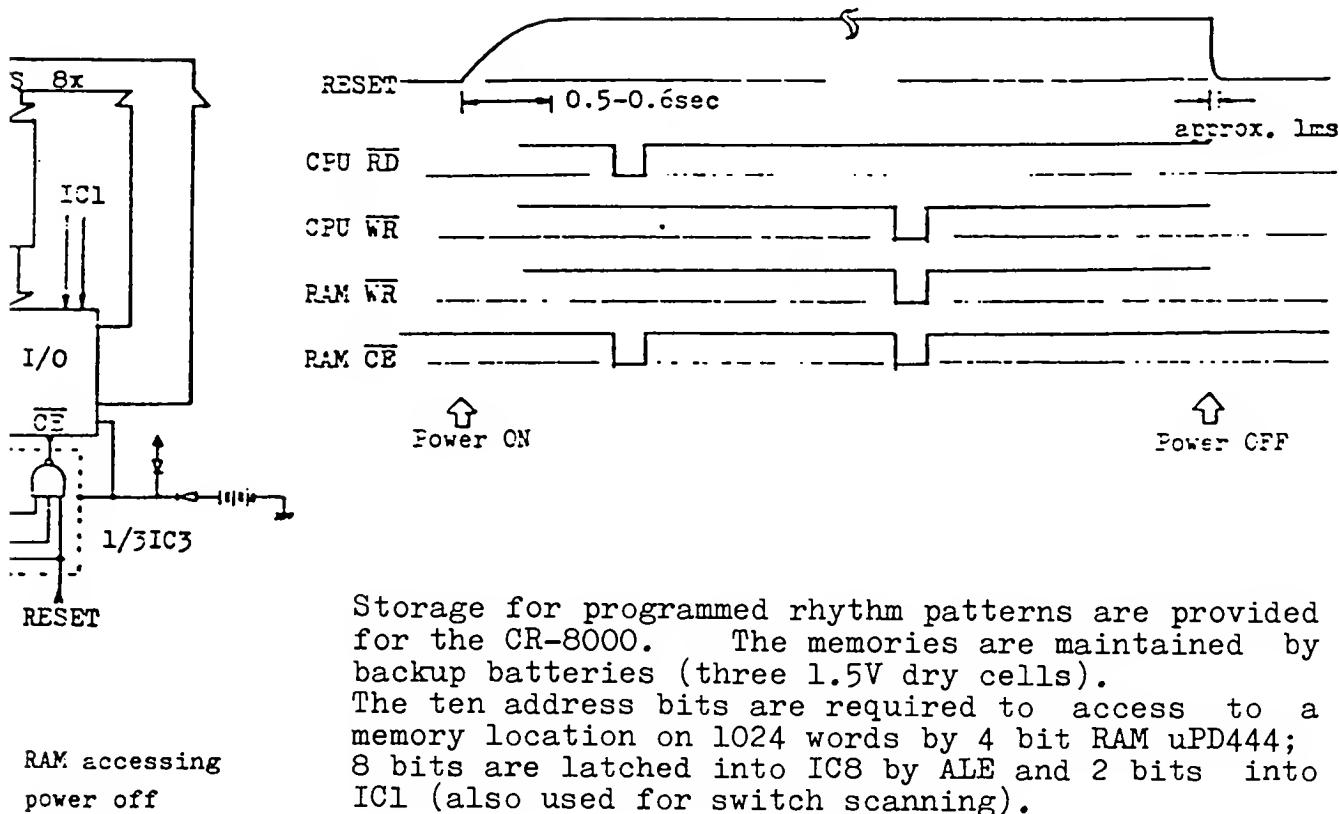
outputs of different summed at BPF after filters.

accomplished by modulate with sawtooth from IC6.

Sounds passing through VCA IC7 are accentuated simultaneously when an accent pulse is applied to Q41 with its amplitude determined by VR8 setting.

## C (CLAVES)

The circuit is designed based on conventional R-C phase oscillator.



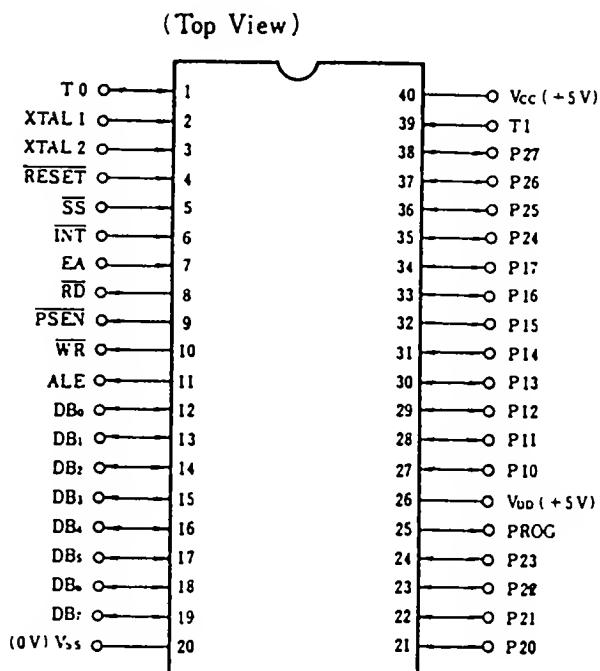
RAM accessing power off

Storage for programmed rhythm patterns are provided for the CR-8000. The memories are maintained by backup batteries (three 1.5V dry cells). The ten address bits are required to access to a memory location on 1024 words by 4 bit RAM uPD444; 8 bits are latched into IC8 by ALE and 2 bits into IC1 (also used for switch scanning).

DEC.8,1981

$\mu$ PD8049C/ $\mu$ PD8048C

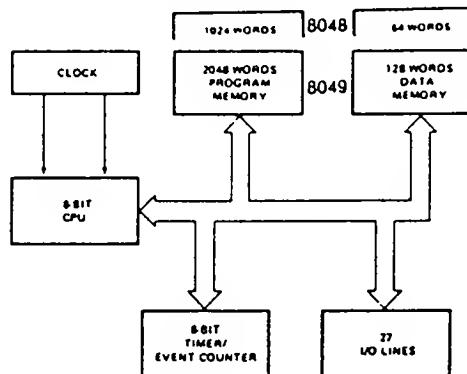
## SINGLE COMPONENT 8-BIT MICROCOMPUTER



**8049**  
2K x 8 ROM  
128 x 8 RAM

**8048**  
1K x 8 ROM/EPROM  
64 x 8 RAM

### BLOCK DIAGRAM



### $\mu$ PD8049C

PIN NAME	PIN NO.	FUNCTION
T $\emptyset$	1	TEMPO CLOCK IN
T1	39	START/STOP SIGNAL IN
INT	6	RESTART SIGNAL IN
DATA BUS	12-19	SWITCH SCANNING OUT/IN LEDs LIGHT OUT TEMPO LED, TRIG OUT MEMORY READ/WRITE (CR-800C only)
PORT 1		TRIGGER OUT FOR VOICE GENERATOR
P10	27	CYMBAL
P11	28	HI TOM
P12	29	OPEN HI-HAT
P13	30	LOW TOM
P14	31	HI-HAT
P15	32	SNARE DRUM
P16	33	BASS DRUM
P17	34	ACCENT
PORT 2		TRIGGER OUT FOR VOICE GENERATOR
P20	21	HI CONGA
P21	22	MIDDLE CONGA
P22	23	LOW CONGA
P23	24	COWBELL
P24	35	CLAVES
P25	36	RIM SHOT
P26	37	HAND CLAP
---	---	---

$\mu$ PD8049C-159

$\mu$ PD8049C-232 (improved version)

The following program bug is eliminated in the -232 version.

#### Condition

SHUFFLE ON with alternate rhythm patterns selected.

INTRO/FILL IN is pushed after the termination of first measure pattern.

When INTRO/FILL IN part ends, CPU delivers rhythm pattern data for the first measure but replaces the first step data only with the one for the second measure.

This is perceptive in RHUMBA, BEGUINE or

$\mu$ PD8048C CR-8000 only

PIN NAME	PIN NO.	FUNCTION
T0	1	NO APPLICATION (KEPT LOW)
T1	39	TEMPO CLOCK IN
INT	6	START/STOP SIGNAL IN
DATA BUS	12 13 14 15 16-19	KEPT HIGH for Internal KEPT LOW program KEPT LOW initialization KEPT LOW NO CONNECTION
PORT 1	P10 P11 P12 P13 P14 P15 P16 P17	27 28 29 30 31 32 33 34
PORT 2	P20-P23 P24 P25 P26 P27	21-24 35 36 37 38

TEMPO DISPLAY (CR-8000 only)

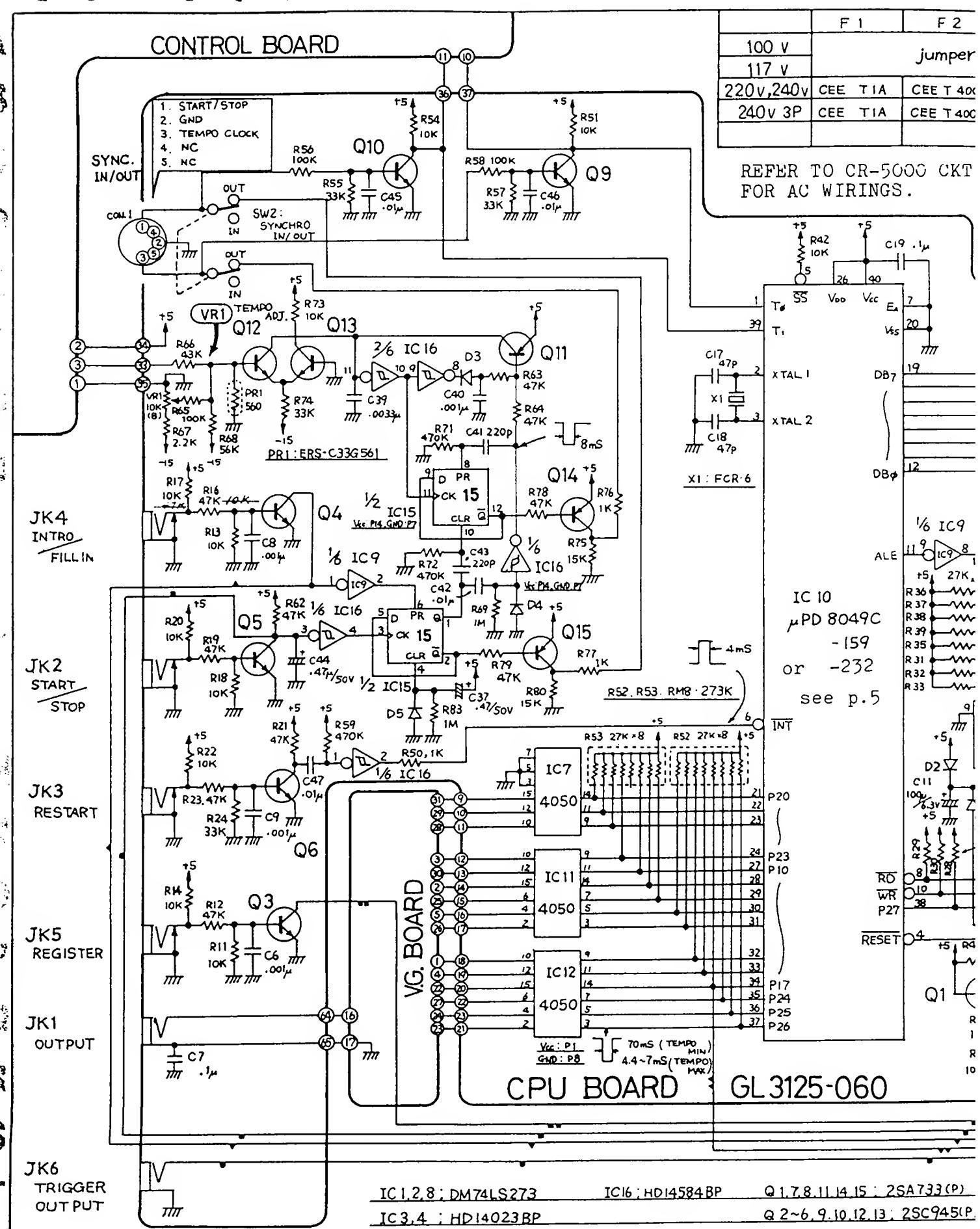
$\mu$ PD8048C IC3 on Control Brd counts Tempo Clocks derived from Q9 on CPU Brd whenever power is being fed to the CR-8000. Since 24 tempo clocks are made equal to one, actual tempo displayed is

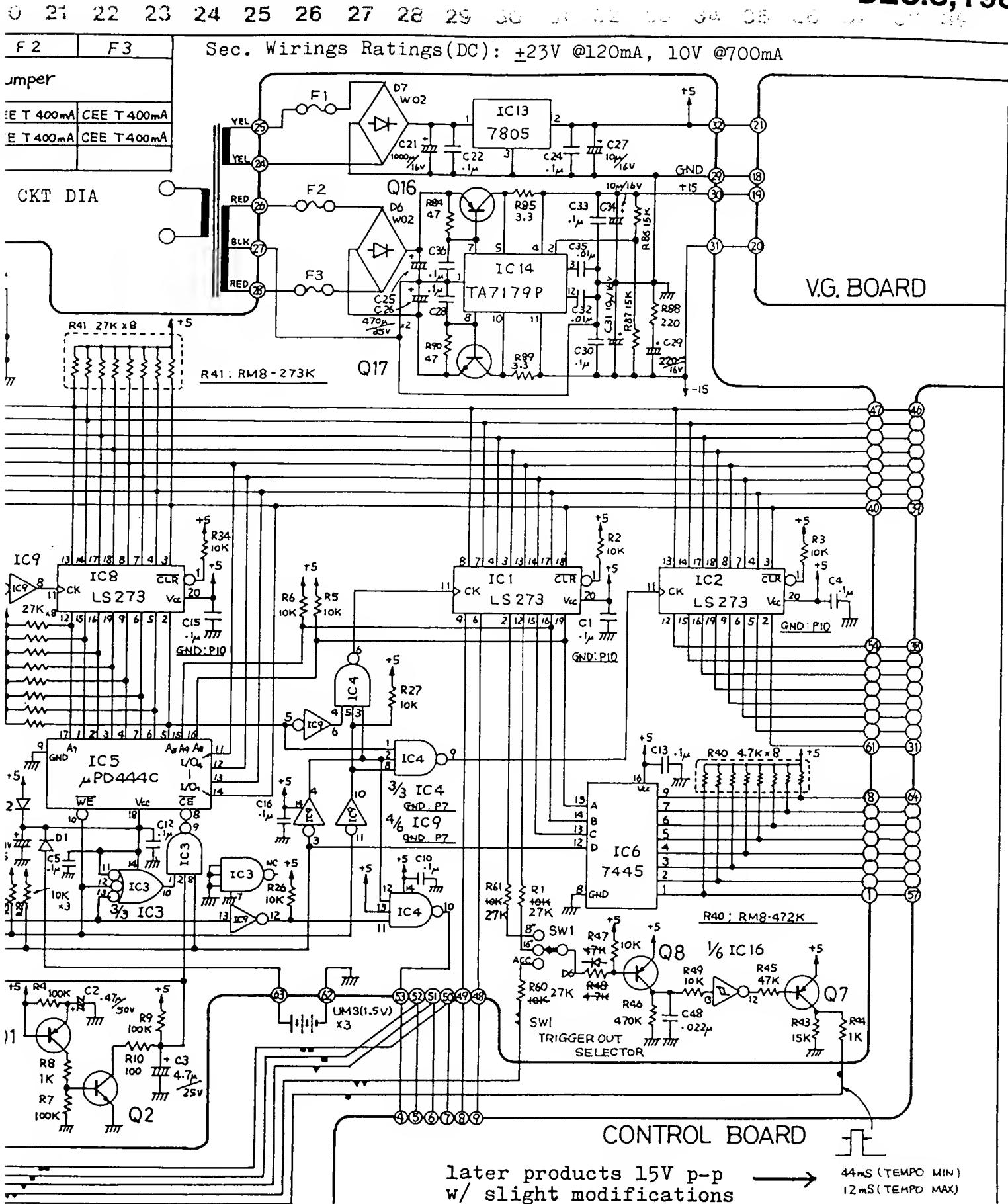
$$\frac{\text{clocks per minute}}{24}$$

CPU performs an equivalent eq. in a short period and drives Q18-Q20 on Control Brd in synchronous with drive signals for 7 segments of display LEDs.

Upon rhythm running INT of CPU IC3 goes and stays negative with which CPU's internal count gate is disabled, then re-started at the first falling edge of the next tempo clock. This count break allows CPU to skip transitional tempo clock that is reset by a start signal.

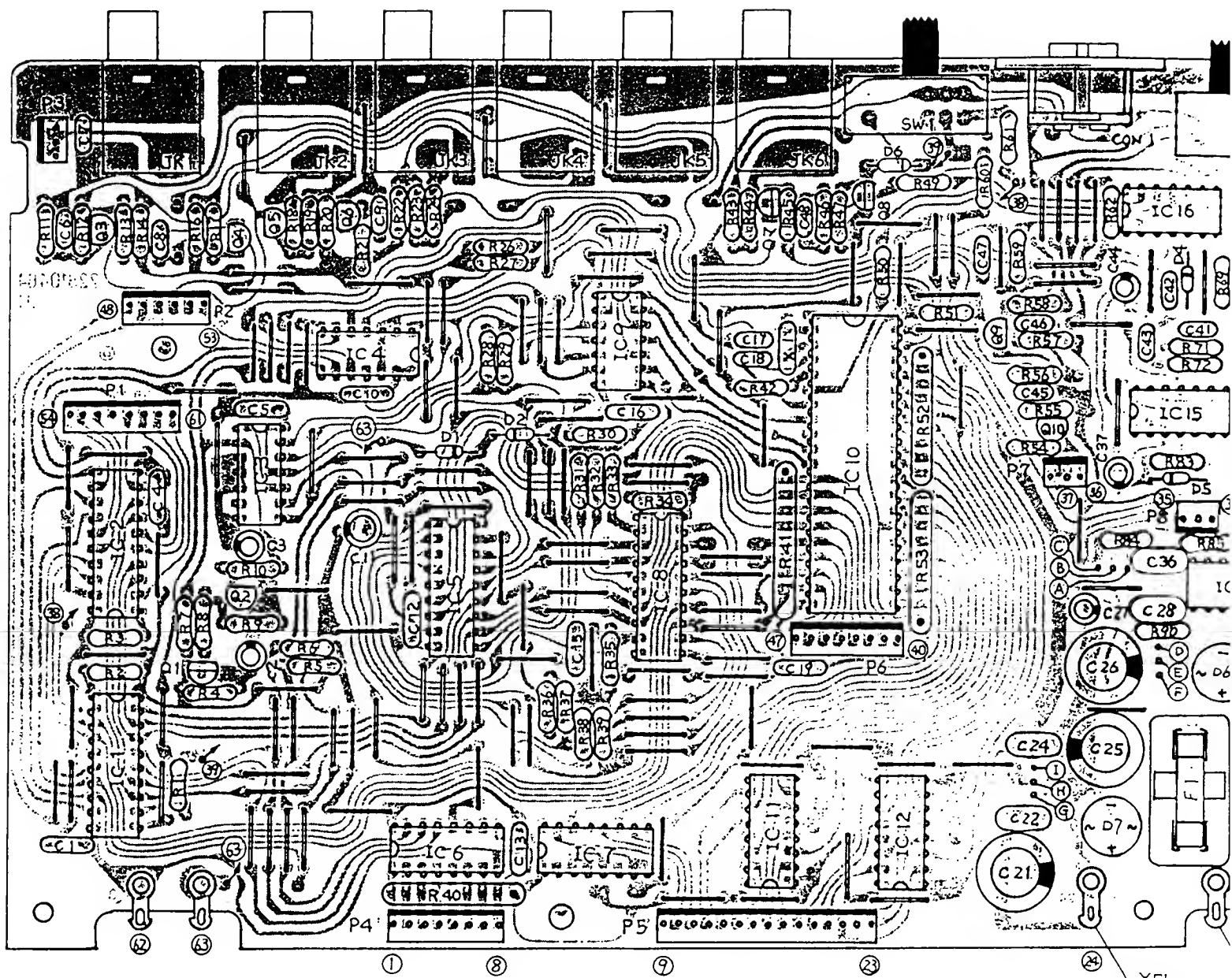
If INT remains high after rhythm running, tempo display varies temporarily.





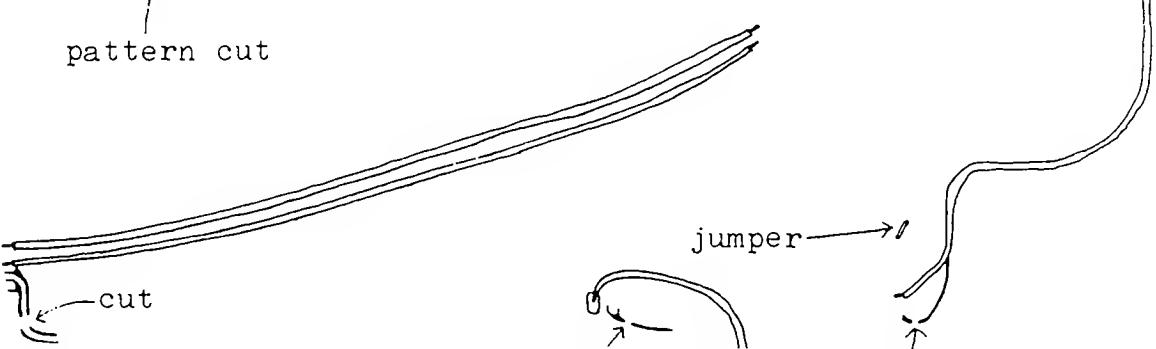
EC.8, 1981

TEMPO

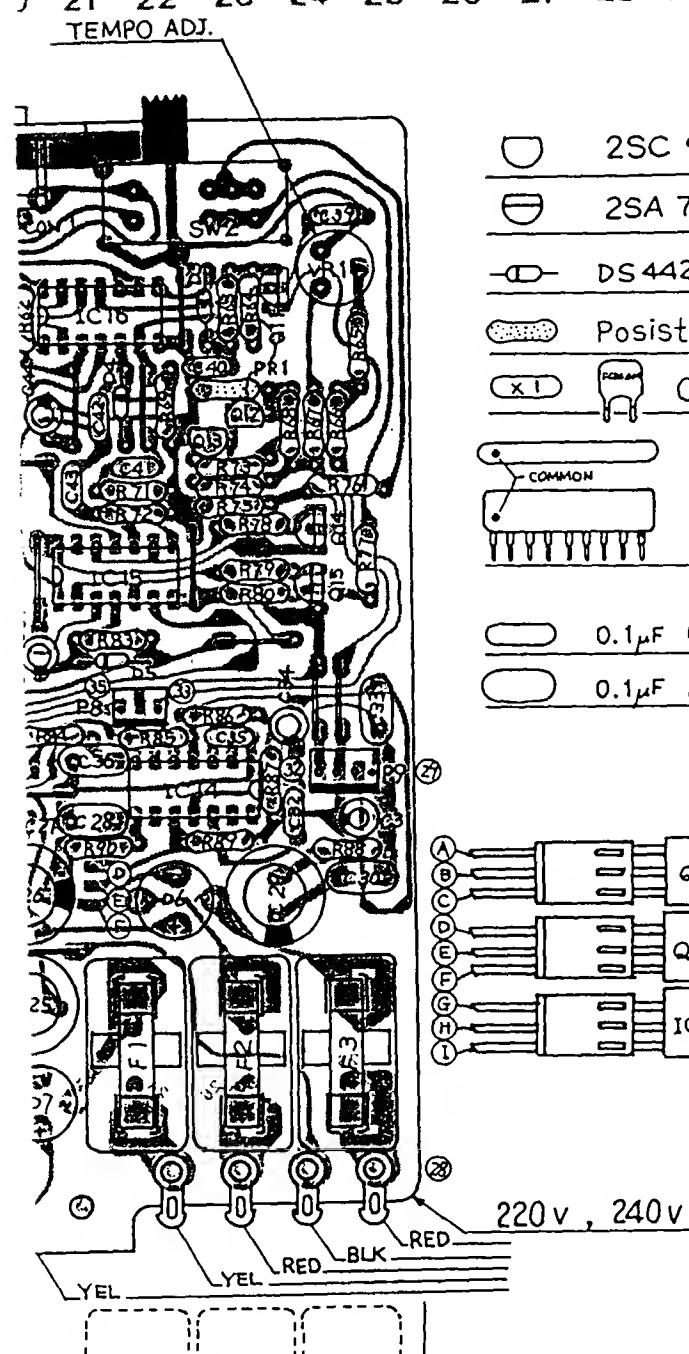


MODIFICATIONS ON FOIL SIDE  
for PCB NO. 2291046400

pattern cut



21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40



- 2SC 945 P
- 2SA 733 P
- DS 442 or 1S 2473 1S 1588
- Posistor ERS-C33G561
- Ceramic Resonator
- Resistor Array  
R40, R41 R52 R53
- 0.1  $\mu$ F Ceramic
- 0.1  $\mu$ F Mylar

**CR-8000  
CPU BOARD**  
**GL3125-060**  
**(731250600)**  
**(pcb 2291046401)**

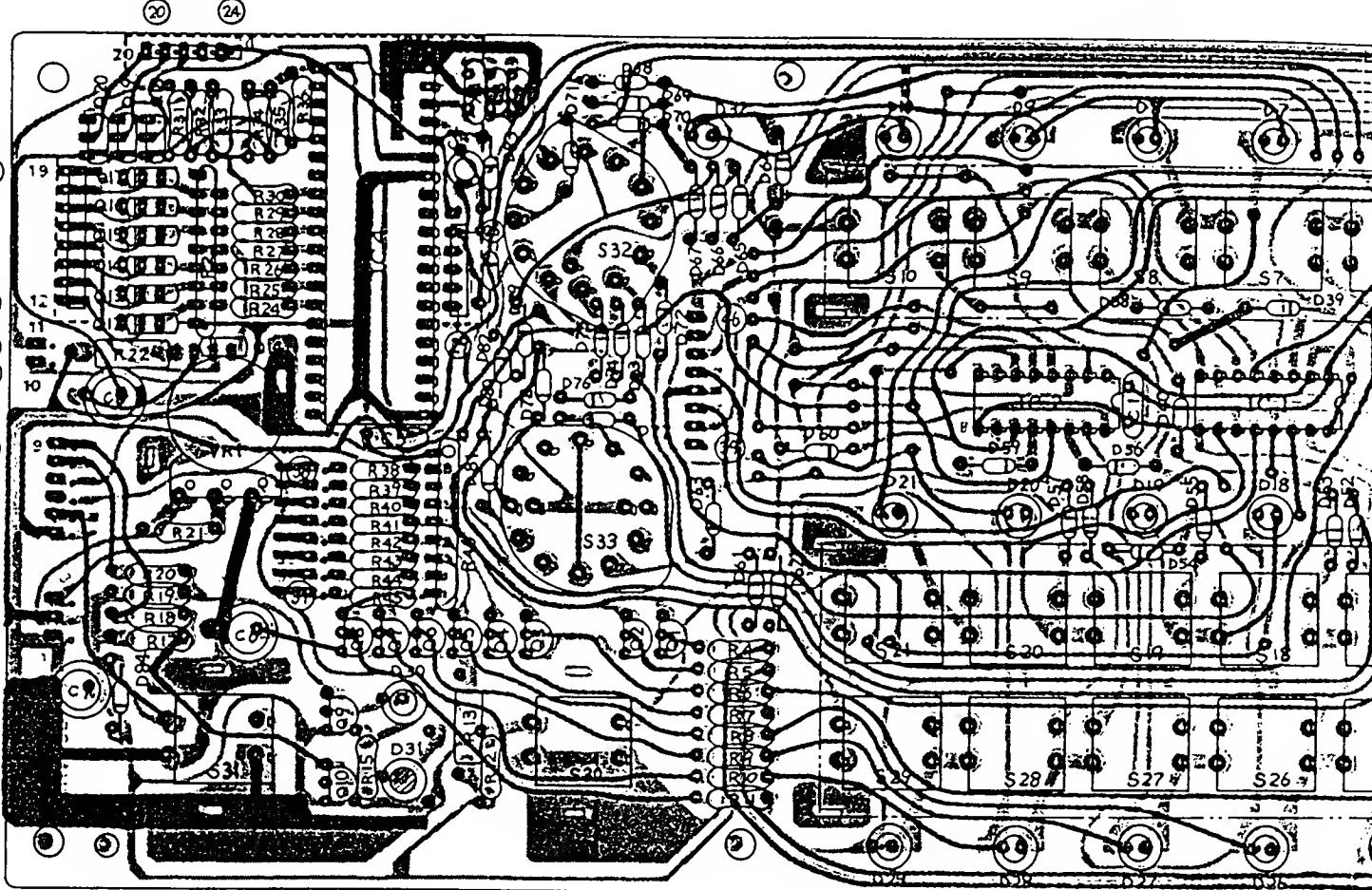
#### CHANGES IN COMPONENTS

Ensure trigger outputs at IC1 when low  $V_{OH}$   
LS273 is used.

R47 47k to 10k  
R48 47k to D6  
R1 10k to 27k  
R61 10k to 27k  
R60 10k to 27k

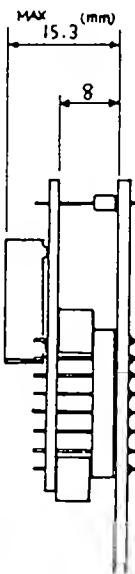
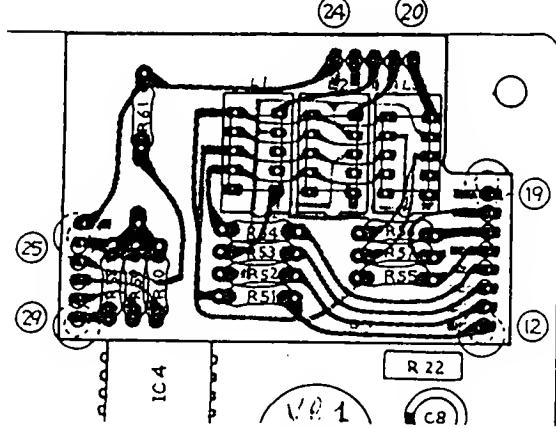
10. *W. C. Gandy, Jr.* (1970) *On the History of Mathematics* (New York: Academic Press).

**CONTROL BOARD GL3125-090 (7312509008) (pcb 2291)**



## LED BOARD

(7312511001)  
(pcb 2291046600)



LED BOARD  
on early products  
pcb 2291046600

without underscore  
Pattern cuts, Jumpers

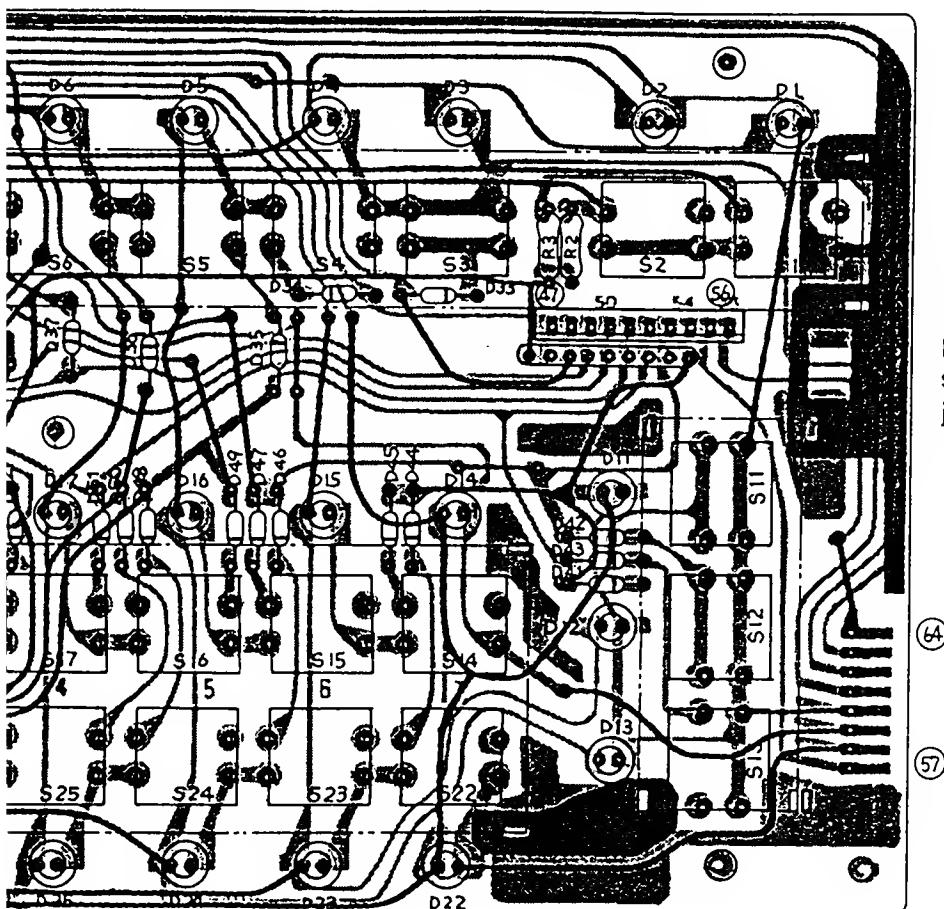
## CR-5000/8000

DEC.8,1981

21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

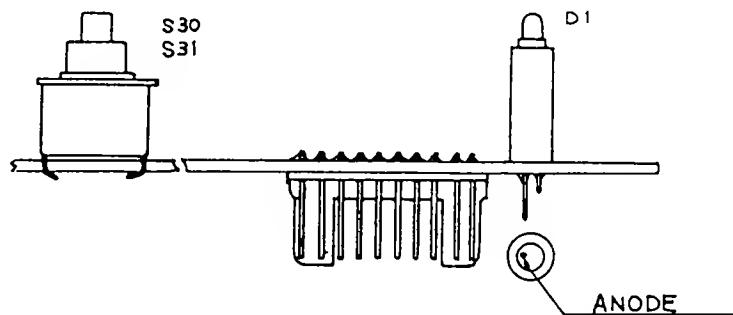
**1046501)** Serial Number 142650 and higher

(Viewed from the rear)

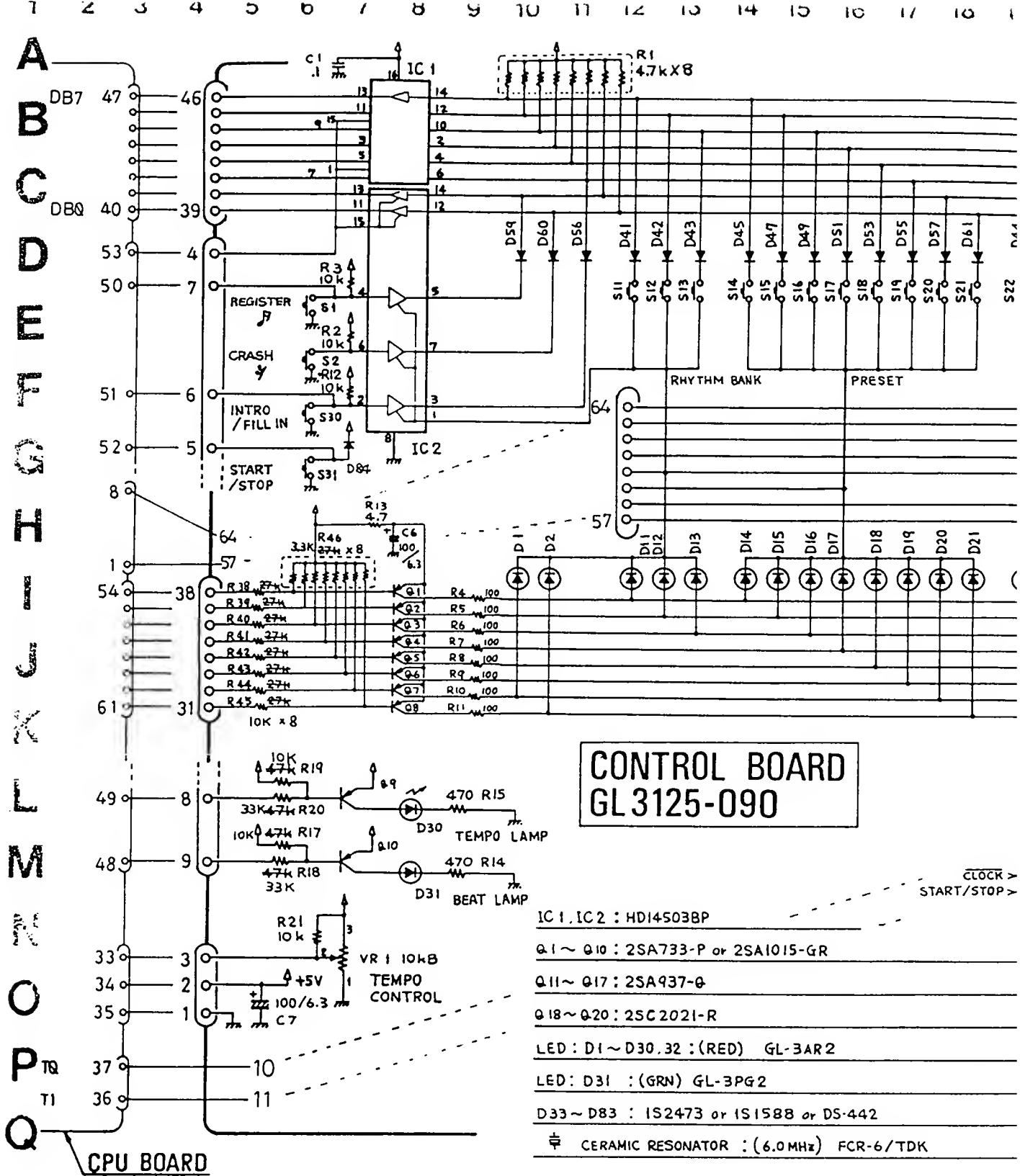


Refer to p.16 for  
pcb 2291046500:  
surface mounting  
jumper wire.

**CR-8000**



- : DS442 or 1S1588, 1S2473
- : 2SA733P or 2SA1015GR
- : 2SA937Q
- : 2SC2021R
- X1 : CERAMIC RESONATOR (6.0MHz) FCR-6
- : LED GL-3PR2 (RED)
- : LED GL-3PG2 (GRN)

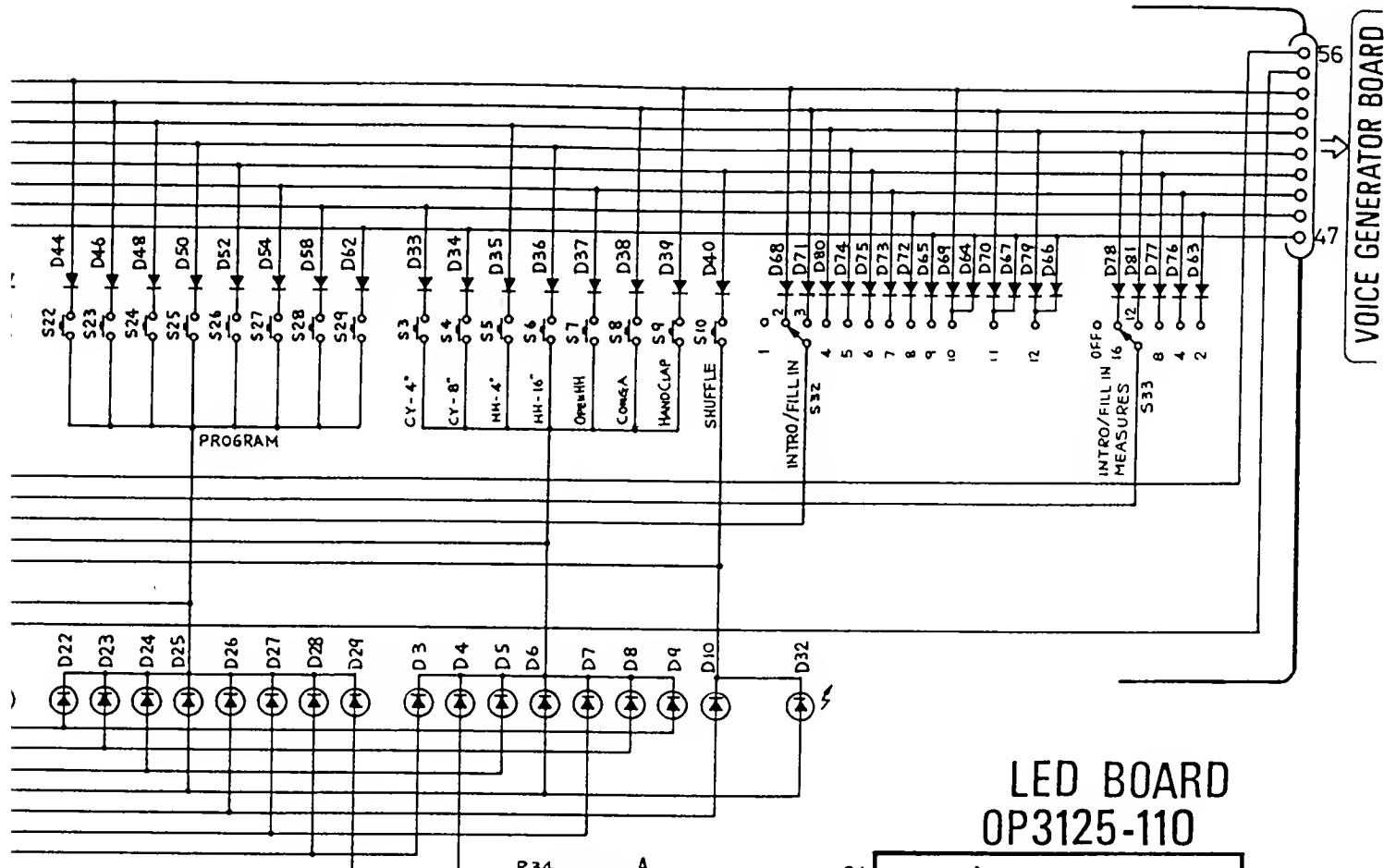
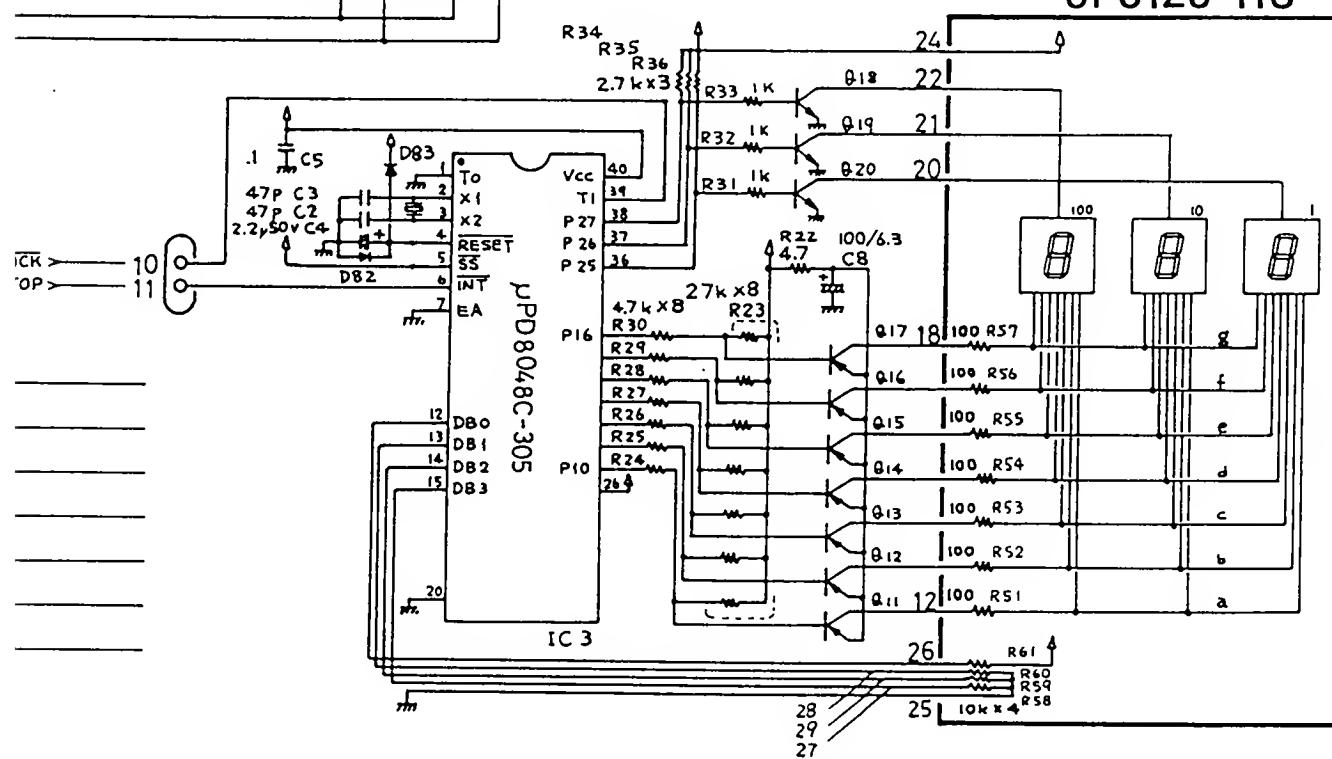


## CHANGES IN RESISTANCE With Serial Number 090900 and up

The changes eliminates possible dim lighting of LEDs due to insufficient power at IC1 or IC2 on CPU board:

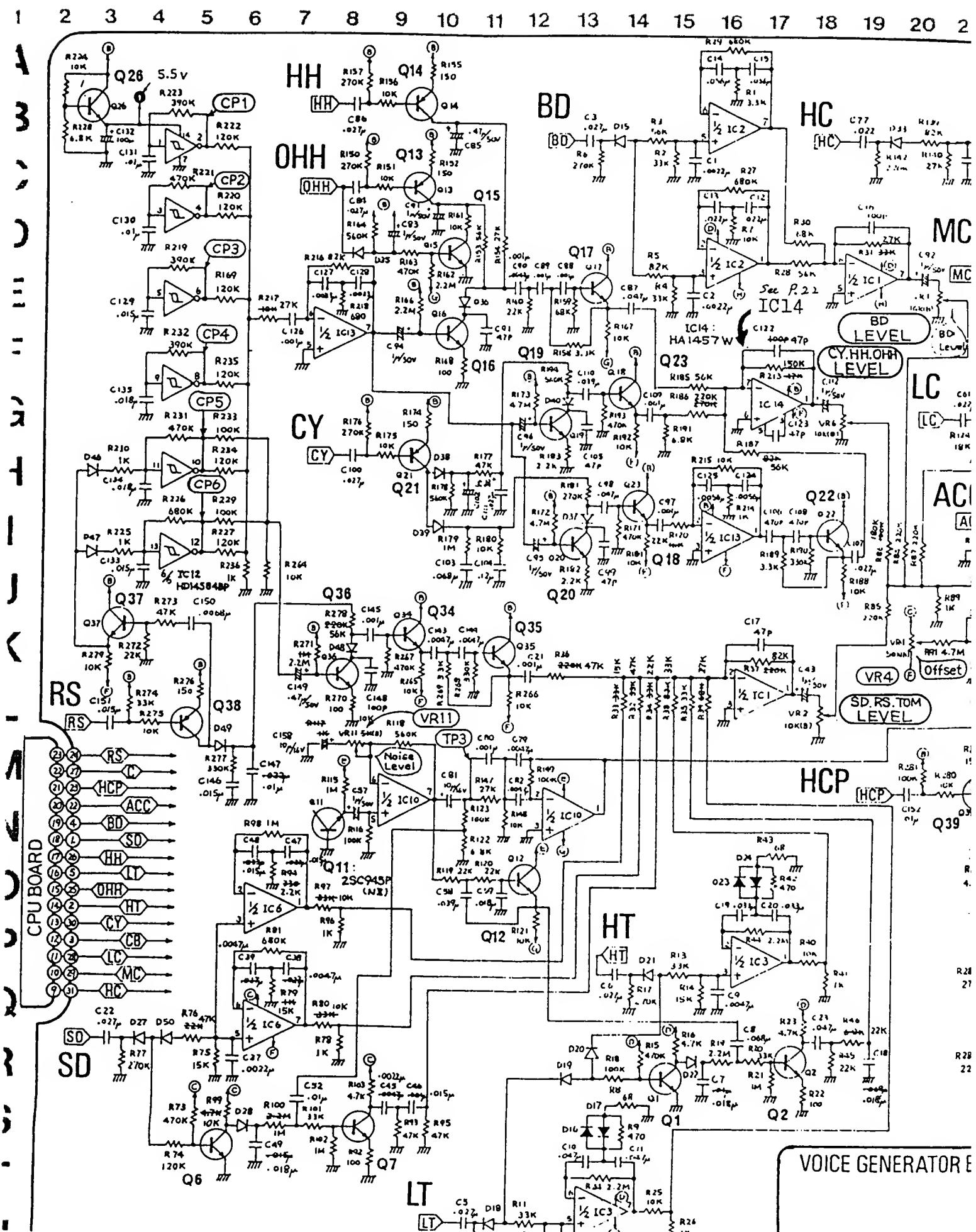
R38-R45: 27k to 10k R17, R19: 47k to 10k R18, R20: 47k to 3  
Resistor Array R46: 27k to 3.3k

19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

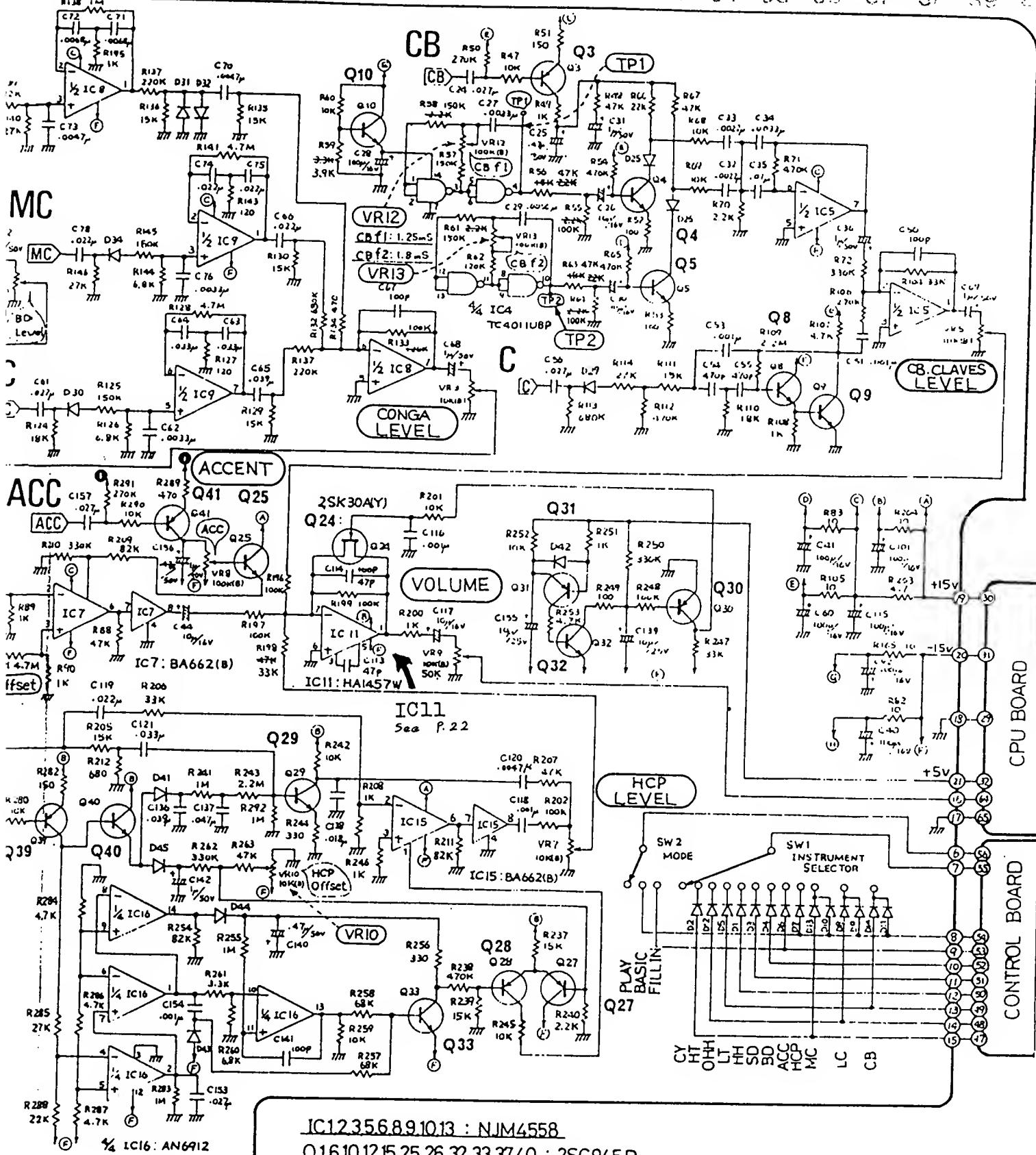
LED BOARD  
OP3125-110

'ficient H level output

## CR-8000 CONTROL



21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 DEC. 8, 1983



IC12356891013 : NJM4558

Q16101215252632333740 : 2SC945P

Q2457~9.16~20.22.23.29.34~36 : 2SC732 TM GR

Q3.13.14.21.27.28.30.31.38.39.41 : 25A733P

D16.17.23.24 : 15188FM

D1~15.18~22.25~50 : DS442, 1S2473 or 1S1588

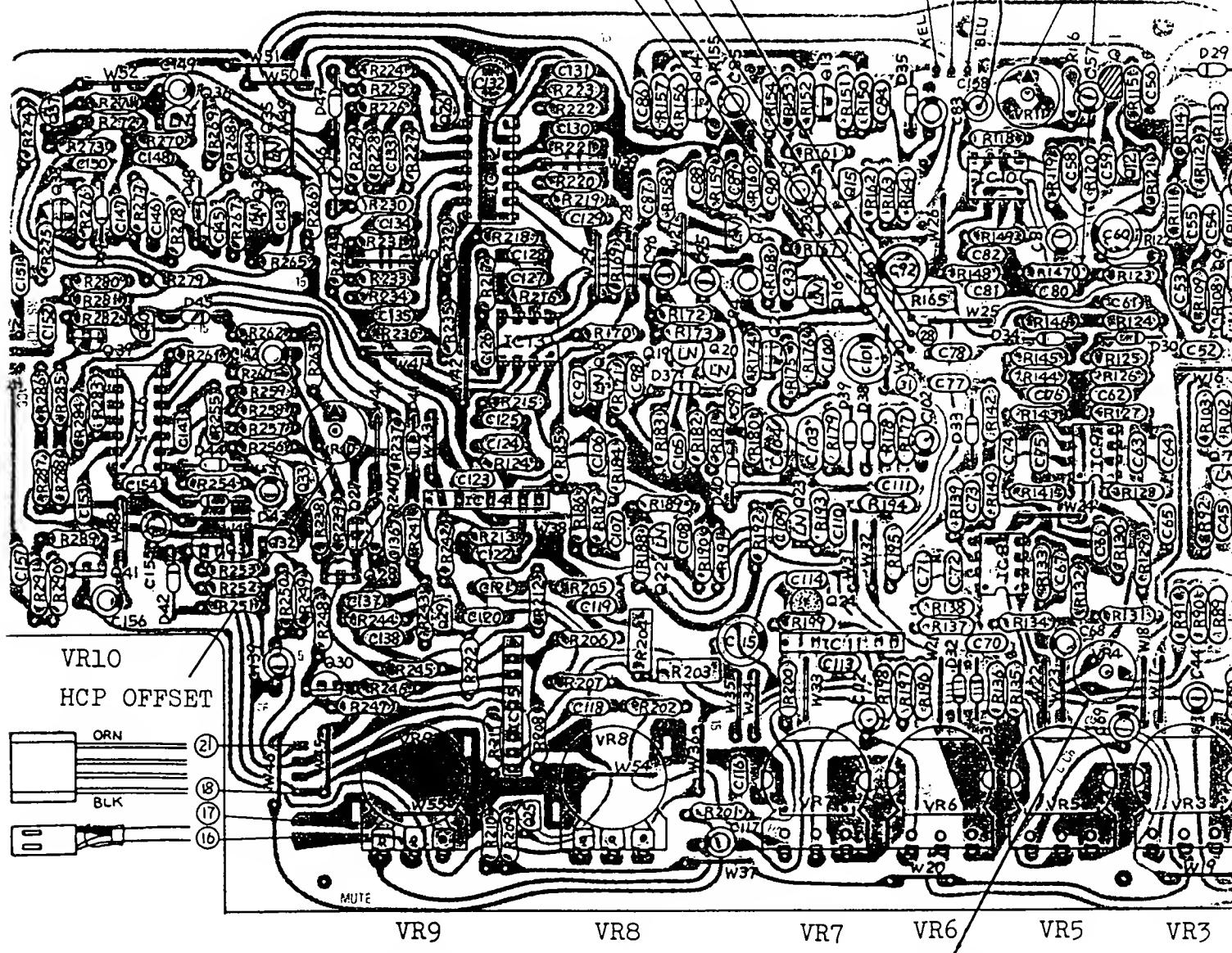
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

early PCB: R117 lkn

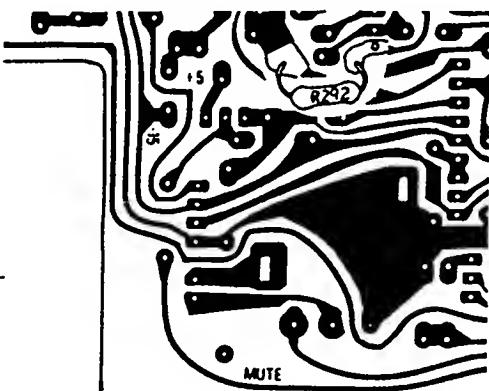
S/N 101300-: C158

VR11 TP-3  
NOISE LEVEL

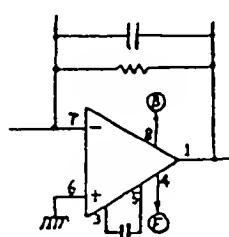
### View from



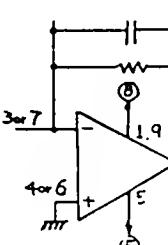
surface  
mounting  
on PCB  
291046301



HA1457W (8 pins) or NJM4558S (



IC11, IC14

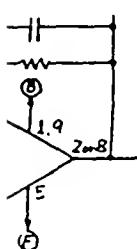
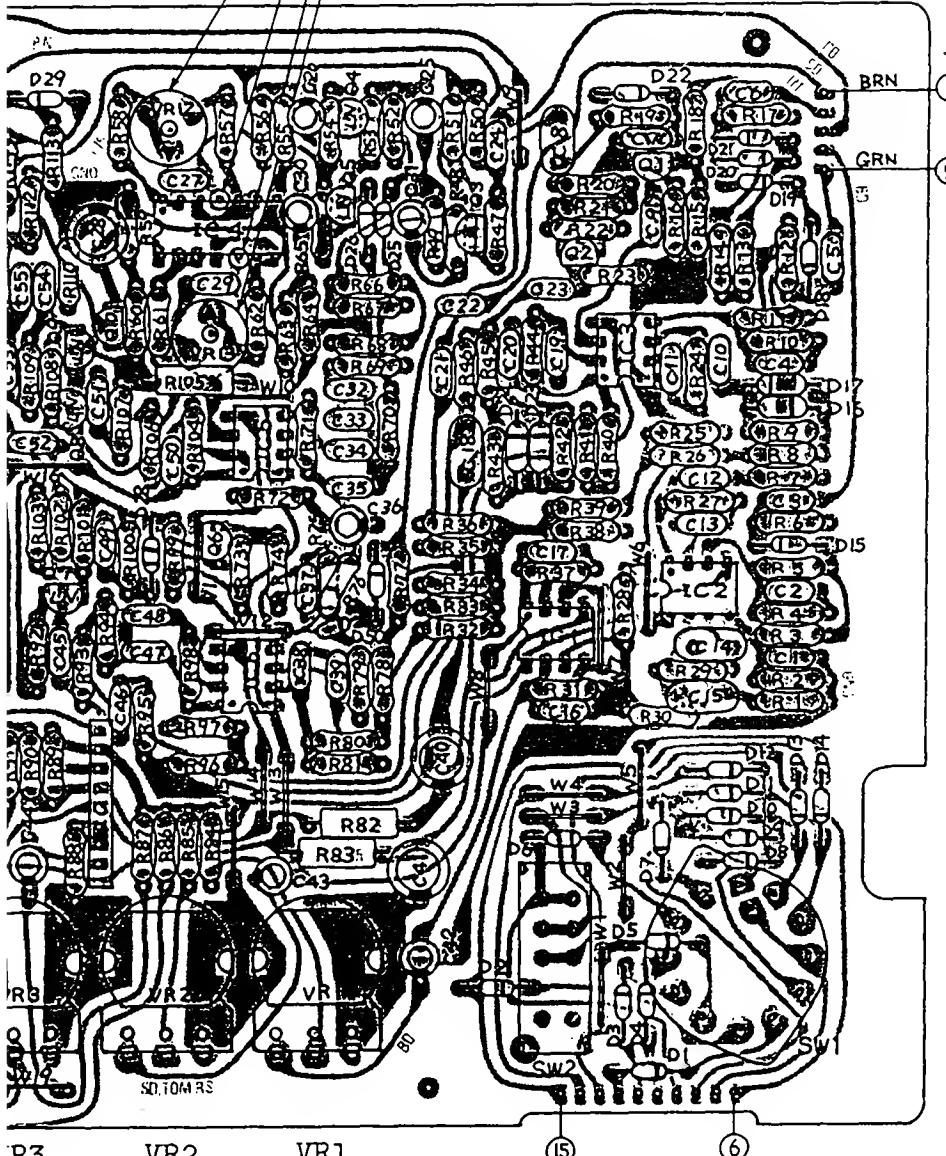


1 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

VR12 TP-1  
CB FREQ

VR13 TP-2  
CB FREQ

from foil side



BS (9 pins) (See p. 22 for detail.)

- 2SC945-P
- 2SC732TM-GR
- 2SA733-P
- ▨ 2SC945-P(NZ)
- ▨ 2SK30A-Y
- DS442, 1S2473 or 1S1588
- 1S188FM

**CR-8000**  
**VOICING BOARD**  
**VG3125-120**  
**(7312512007)**  
**(pcb 2291046302)**

## CHANGES IN COMPONENTS

with S/N 090900  
VR9 from 10k to 50k  
Eliminates whizz sound  
upon power off.

with S/N 101300  
R198(HCP) 47k to 33k

with S/N 111700  
R55,56,58,61,63,64  
resistances are increased  
to limit currents into  
IC4. This modification is  
mandatory when replacing  
defective IC4.

ALSO SEE CR-5000 VG BRD  
LAYOUT FOR OTHER MODIFI-  
CATIONS.

# ADJUSTMENTS

## CPU BOARD

RAM BACK UP BATTERIES (CR-8000 only)

Power switch must be turned OFF.

Connect 100 ohms across pins 18 (Vcc) and 9 (GND) of RAM IC5 or shunt meter (scope or voltmeter) inputs with 100 ohms. Confirm approx. 4V at pin 18.

## TEMPO CLOCK

Allow at least 10 minutes for circuit thermal stabilization.

### CR-5000

Connect scope to pin 1 of CPU (TP-1). Set scope time base to 5ms/div.

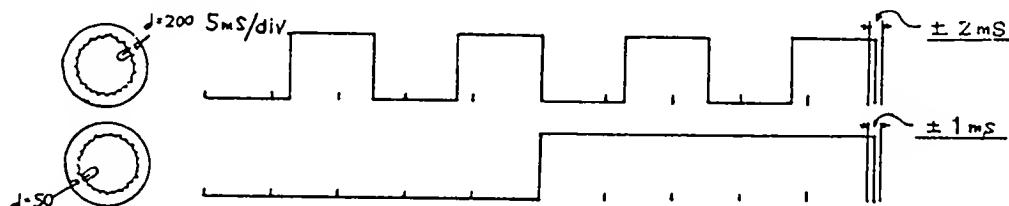
With TEMPO set at 200 adjust VR1 for 12.5ms/cycle (50ms/4 cycles).

Reset TEMPO to 50 and confirm that 1 cycle is  $50 \pm 1\text{ms}$ . If exceeds this limit, readjust VR1 for 1ms at the sacrifice of  $\pm 2\text{ms}$  error at TEMPO 200.

### CR-8000

Turning TEMPO across its travel, confirm TEMPO DISPLAY; factory set ranges from  $33 \pm 2$  to  $375 \pm 5\%$ . Adjust VR1 as required.

NOTE: TEMPO = 
$$\frac{2500}{\text{period of one tempo clock cycle (ms)}}$$



## VOICE BOARD

### NOISE

Connect scope (1V/div, time base relatively slow) to TP-3.

Adjust VR11 for 2V p-p when measured at rather dense peaks.

### CB

Connect scope to TP-1. Adjust VR12 for 1.25ms/cycle.

Connect scope to TP-2. Adjust VR13 for 1.8ms/cycle.

### CY

See table right. Probing CP1-CP6 of oscillators IC6, confirm frequency ratios between adjacent two; they should be in 1.1-1.4 steps. Note that two oscillators generating on too close frequency will sound beating cymbal which can be eliminated by tailoring R and C listing on the table.

### OFFSET

Controls set up - All VOICE LEVELs: FCCW; VOLUME, ACCENT: MAX; RYTHM: DISCO Start the rythm. Monitoring through OUTPUT jack (scope or amp), adjust VR4 for minimum thump.

## HCP (CR-8000 only)

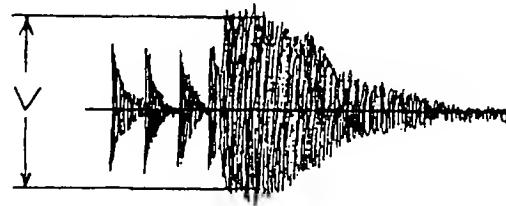
Controls set up - HCP VOICE LEVEL: FCW; VOLUME: MAX; ARRANGER: HAND CLAP

Connect scope V IN to OUTPUT jack and H (EXT) to HCP trig terminal 23.

Adjust VR10 for the below:

Serial number up to 101299 1V p-p

Serial number 101300 and up 2V p-p



		FREQUENCY (mS)(Hz)									VOICE LEVEL CONTROL AT HOT TERMINAL						OUTPUT JACK			
		CHECK POINT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V <sub>p-p</sub> )	DECAY TIME (mS)	AMPLITUDE (V <sub>p-p</sub> )
BD	H	IC2 PIN 1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	6.7	8.0	9.6	77	96	115	1.2		
	L	IC2 PIN 7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110									
SD	H	IC6 PIN 1	3.5 (286)	3.0 (333)	2.5 (400)	4.7	5.6	6.5	8	10	12	10.8	13.0	15.6	58	72	86	1.7		
	L	IC6 PIN 7	5.1 (196)	4.4 (227)	3.8 (266)	16.8	20.0	23.2	28	34	40									
LT		IC3 PIN 7	10.9 (91.7)	9.4 (106)	8.0 (124)	24	27	28												
HT		IC3 PIN 1	7.6 (132)	6.6 (152)	5.6 (177)	24	27	28												
LC		IC9 PIN 7	5.8 (172)	5.0 (200)	4.3 (234)	24	27	28												
MC		IC9 PIN 1	3.9 (256)	3.4 (294)	2.9 (343)	24	27	28												
HC		IC8 PIN 1	1.67 (599)	1.45 (690)	1.24 (807)	24	27	28												
CB		TP1,VR12 TP2,VR13			1.25 (1.80) (200)(555)															
C		Q9 COLLECTOR	0.49(2.01K)	0.43(2.33K)	0.37(2.72K)															
HCP		VR10																		

	CHECK POINT	R (kΩ)	C (μF)	FREQUENCY (mS)(Hz)			RS	CY	HH	OHH
				MIN	TYP	MAX				
RS	CP 1	R223 390	C131 0.01	1.58 (631)	1.26 (794)					
	CP 2	R221 470	C130 0.01		1.54 (647)					
CY	CP 3	R219 390	C129 0.015		1.91 (524)					
	CP 4	R232 390	C125 0.018		2.25 (444)					
OHH	CP 5	R231 470	C124 0.019		2.72 (368)					
	CP 6	R228 680	C133 0.015	4.20 (238)	3.53 (283)					

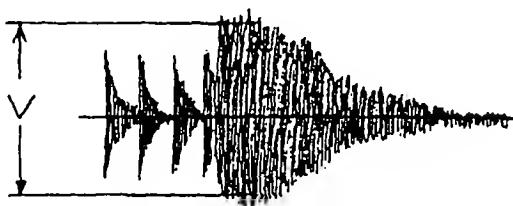
Ref. set up  
VOICE LEVEL, VOLUME: MAX  
ACCENT : MIN  
(@ MAX, add 12dB to each:  
four times MIN.)

		FREQUENCY (mS)(Hz)									VOICE LEVEL CONTROL AT HOT TERMINAL						OUTPUT JACK			
		CHECK POINT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V <sub>p-p</sub> )	DECAY TIME (mS)	AMPLITUDE (V <sub>p-p</sub> )
BD	H	IC2 PIN 1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	7.2	9.0	10.8	77	96	115	1.5		
	L	IC2 PIN 7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110									
SD	H	IC6 PIN 1	4.4 (227)	3.8 (263)	3.2 (308)	24	27	28	54	64	74	9.6	12.0	14.4	58	72	86	1.7		
	L	IC6 PIN 7	5.1 (196)	4.4 (227)	3.8 (266)				30	40	50									
LT		IC3 PIN 7	10.9 (91.7)	9.4 (106)	8.0 (124)							7.2	9.0	10.8	160	200	240	1.5		
		IC3 PIN 1	7.6 (132)	6.6 (152)	5.6 (177)															
HT		IC9 PIN 7	5.8 (172)	5.0 (200)	4.3 (234)							5.6	7.0	8.4	120	150	180	1.0		
		IC9 PIN 1	3.9 (256)	3.4 (294)	2.9 (343)															
LC		IC8 PIN 1	1.67 (599)	1.45 (690)	1.24 (807)							6.4	8.0	9.6	136	170	200	1.3		
		TP1,VR12 TP2,VR13			1.25 (1.80) (200)(555)															
MC		Q9 COLLECTOR	0.49(2.01K)	0.43(2.33K)	0.37(2.72K)							2.4	3.0	3.6	80	100	120	0.5		
		VR10																		

Controls set up - HCP VOICE LEVEL: FCW; VOLUME: MAX; ARRANGER: HAND CLAP  
 Connect scope V IN to OUTPUT jack and H (EXT) to HCP trig terminal 23.

Adjust VR10 for the below:

Serial number up to 101299 1V p-p  
 Serial number 101300 and up 2V p-p



		VOICE LEVEL CONTROL AT HOT TERMINAL												OUTPUT JACK						
		FREQUENCY (mS)(Hz)						AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			AMPLITUDE (V <sub>p-p</sub> )
		CHECK POINT		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
BD	H	IC2 PIN 1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	6.7	8.0	9.6	77	96	115	1.2		
	L	IC2 PIN 7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110									
SD	H	IC6 PIN 1	3.5 (286)	3.0 (333)	2.5 (400)	4.7	5.6	6.5	8	10	12	10.8	13.0	15.6	58	72	86	1.7		
	L	IC6 PIN 7	5.1 (196)	4.4 (227)	3.8 (266)	16.8	20.0	23.2	28	34	40									
LT	IC3 PIN 7	10.9 (91.7)	9.4 (106)	8.0 (124)	24	27	28				7.0	8.8	10.6	160	200	240	1.3			
HT	IC3 PIN 1	7.6 (132)	6.6 (152)	5.6 (177)	24	27	28				4.6	6.0	7.4	120	150	180	1.0			
LC	IC9 PIN 7	5.8 (172)	5.0 (200)	4.3 (234)	24	27	28				6.4	8.0	9.6	136	170	200	1.3			
MC	IC9 PIN 1	3.9 (256)	3.4 (294)	2.9 (343)	24	27	28				2.2	2.8	3.4	80	100	120	0.4			
HC	IC8 PIN 1	1.67 (599)	1.45 (690)	1.24 (807)	24	27	28				3.4	4.3	5.1	12	15	18	0.6			
CB	TP1,VR12 TP2,VR13			1.25 (1.80) (800)(555)							1.1	1.3	1.6	29	36	43	1.3			
C	Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5			
HCP	VR10										0.4	0.6	0.8	72	90	108	2.0			

	CHECK POINT	R (kΩ)	C (μF)	FREQUENCY (mS)(Hz)		
				MIN	TYP	MAX
RS	CP 1	R223 390	C131 0.01	1.58 (631)	1.26 (794)	
	CP 2	R221 270	C130 0.01		1.56 (547)	
CY	CP 3	R221 390	C135 0.015		1.91 (524)	
	CP 4	R232 390	C135 0.018		2.25 (444)	
HH	CP 5	R231 470	C134 0.018		2.72 (368)	
	CP 6	R226 680	C133 0.015	4.20 (238)	3.53 (283)	

RS	18.4	23	27.6	24	30	36	2.6
CY	6.3	7.6	9.1	300	380	450	1.2
HH	5.8	7.0	8.4	59	74	89	1.1
OHH	5.2	7.0	8.4	240	300	360	1.1

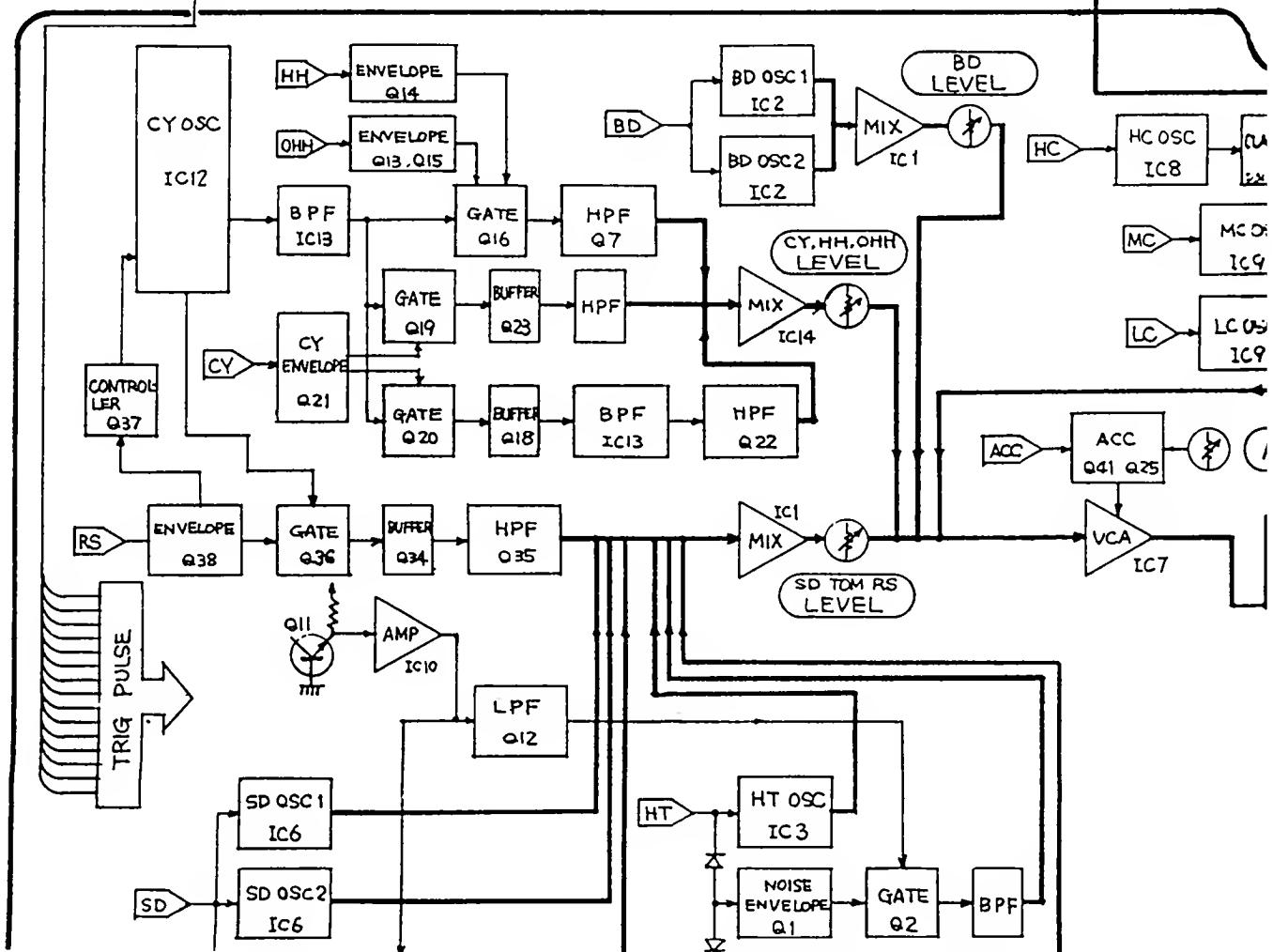
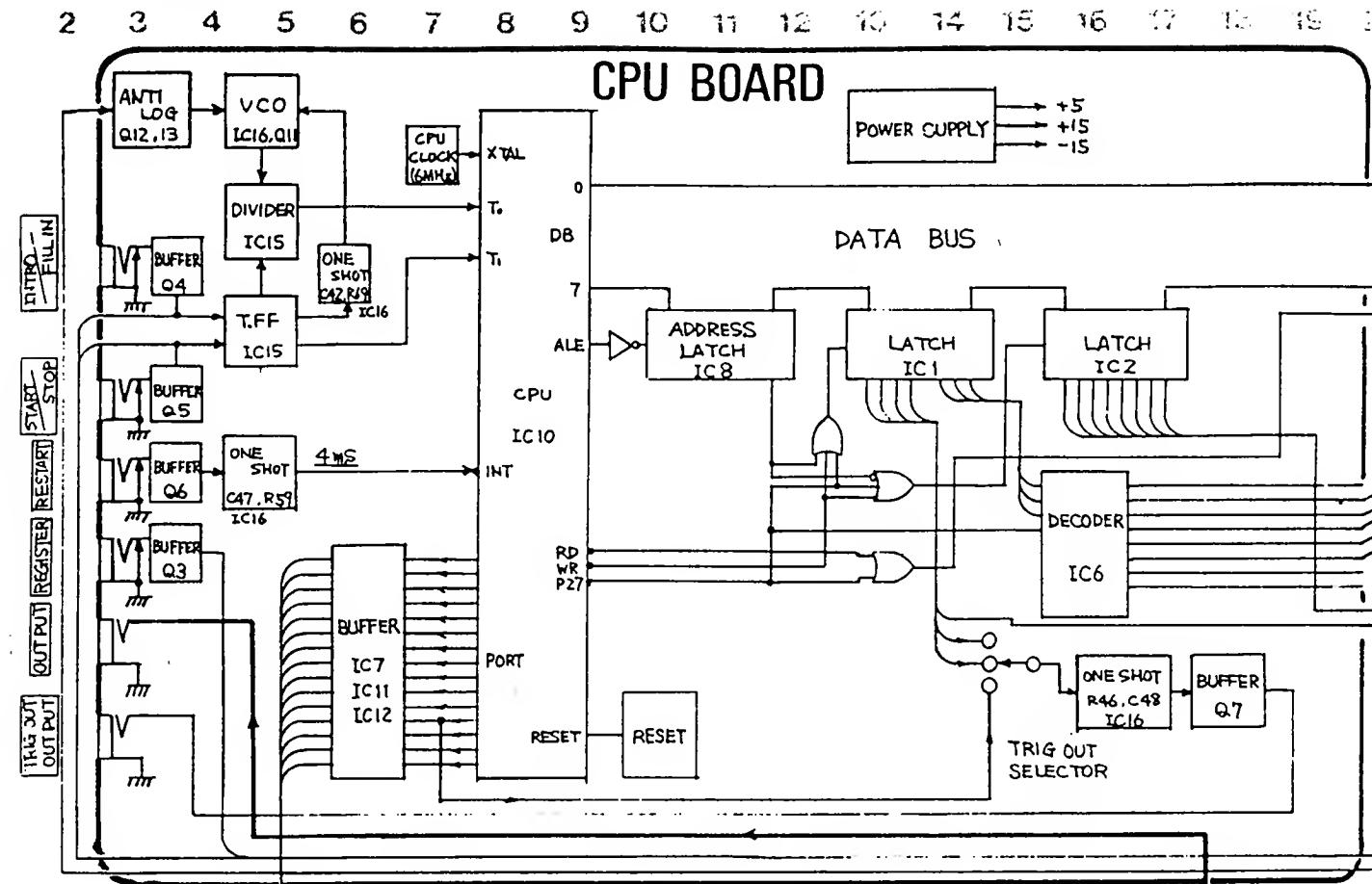
Ref. set up  
 VOICE LEVEL, VOLUME: MAX  
 ACCENT : MIN  
 (@ MAX, add 12dB to each:  
 four times MIN.)

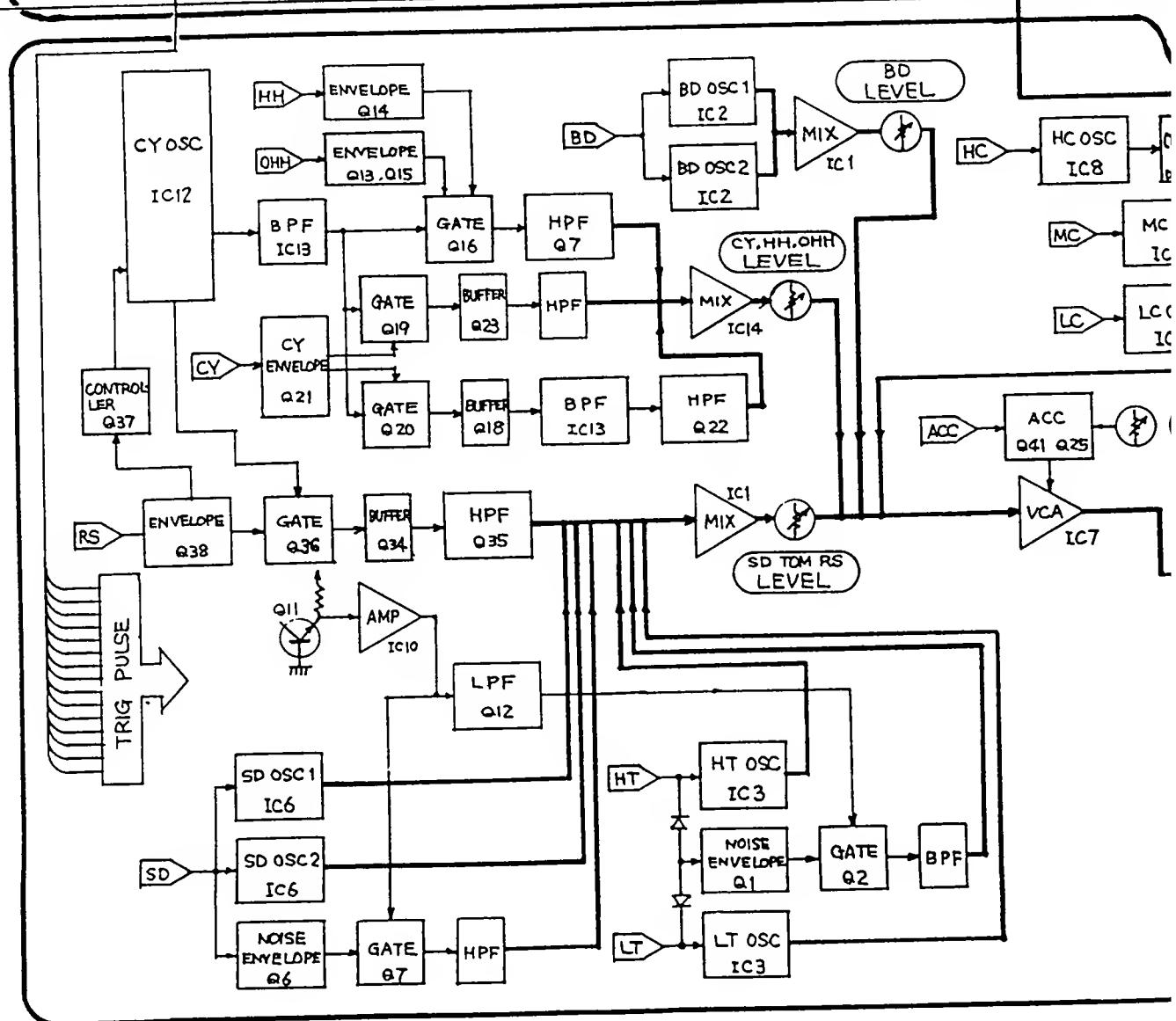
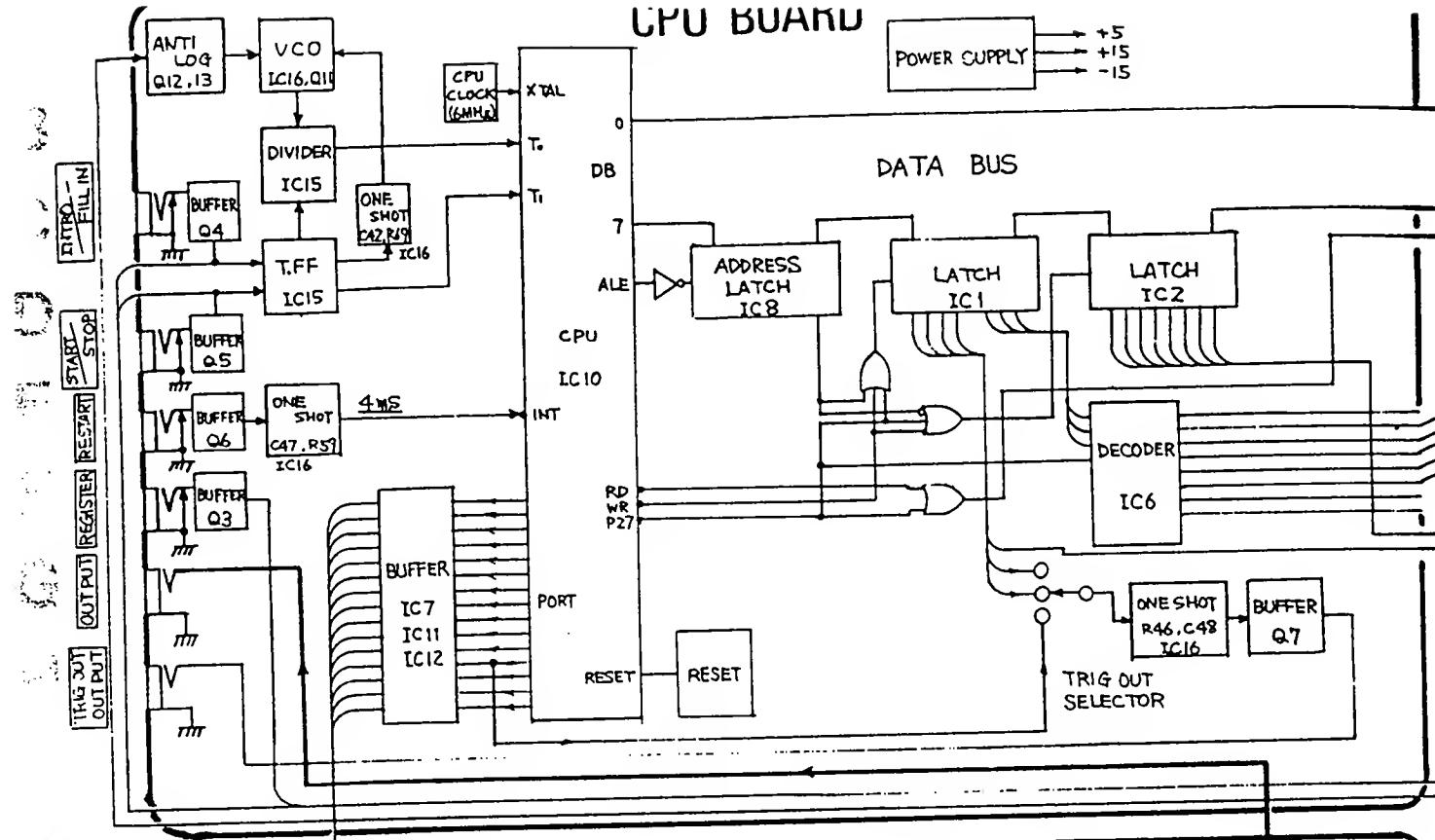
		VOICE LEVEL CONTROL AT HOT TERMINAL												OUTPUT JACK						
		FREQUENCY (mS)(Hz)						AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			AMPLITUDE (V <sub>p-p</sub> )			DECAY TIME (mS)			AMPLITUDE (V <sub>p-p</sub> )
		CHECK POINT		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
BD	H	IC2 PIN 1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	7.2	9.0	10.8	77	96	115	1.5		
	L	IC2 PIN 7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110									
SD	H	IC6 PIN 1	4.4 (227)	3.8 (263)	3.2 (308)	24	27	28	54	64	74	9.6	12.0	14.4	58	72	86	1.7		
	L	IC6 PIN 7	5.1 (196)	4.4 (227)	3.8 (266)				30	40	50									
LT	IC3 PIN 7	10.9 (91.7)	9.4 (106)	8.0 (124)							7.2	9.0	10.8	160	200	240	1.5			
HT	IC3 PIN 1	7.6 (132)	6.6 (152)	5.6 (177)							5.6	7.0	8.4	120	150	180	1.0			
LC	IC9 PIN 7	5.8 (172)	5.0 (200)	4.3 (234)							6.4	8.0	9.6	136	170	200	1.3			
MC	IC9 PIN 1	3.9 (256)	3.4 (294)	2.9 (343)							2.4	3.0	3.6	80	100	120	0.5			
HC	IC8 PIN 1	1.67 (599)	1.45 (690)	1.24 (807)							3.4	4.3	5.1	12	15	18	0.6			
CB	TP1,VR12 TP2,VR13			1.25 (1.80) (800)(555)							1.1	1.3	1.6	29	36	43	1.3			
C	Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5			
HCP	VR10										0.4	0.6	0.8	72	90	108	1.0			

CR-5000 S/N up to 101399  
 CR-8000 S/N up to 101299

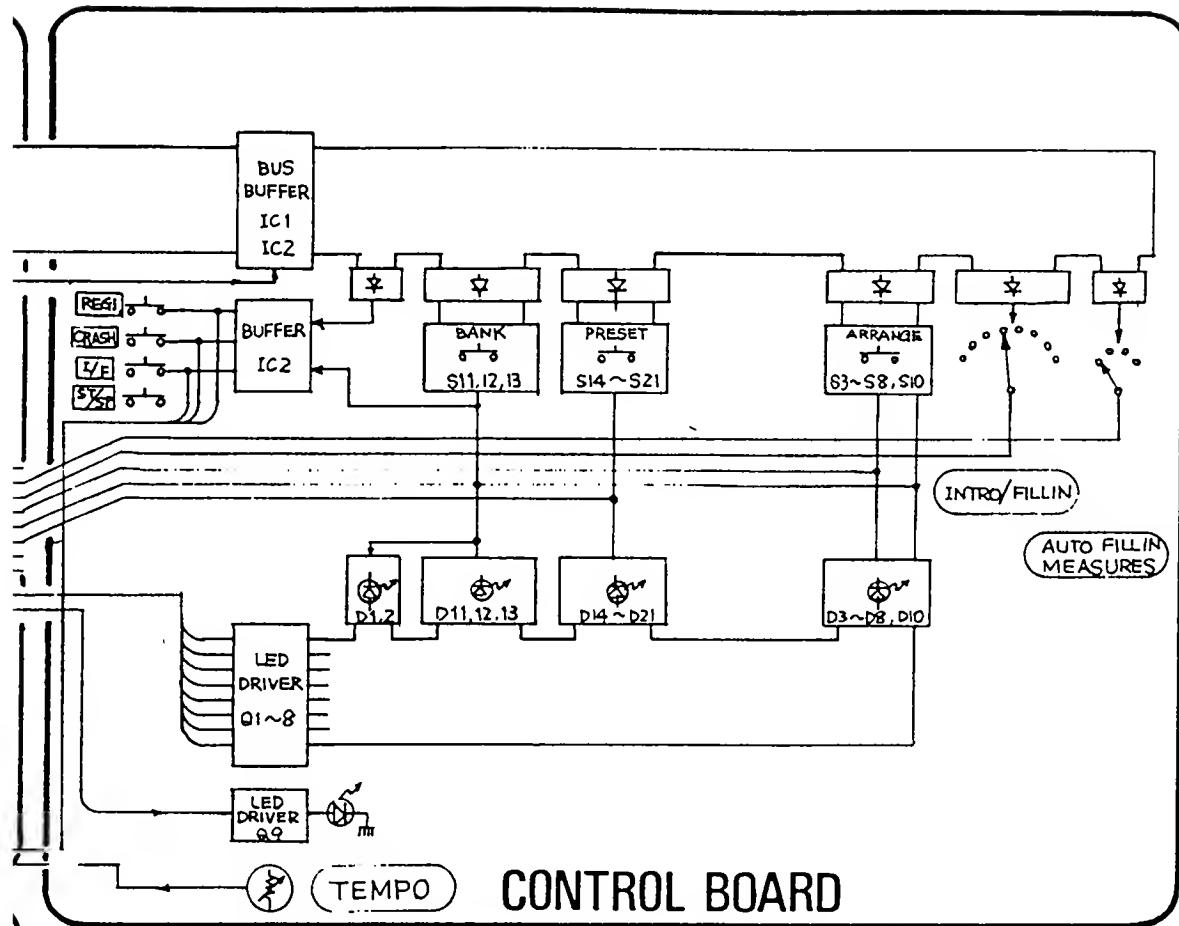
See table above for  
 RS, CY, HH and OHH frequencies.

RS	10	13	16	24	30	36	1.5
CY	2.5	3.5	4.5	300	380	450	1.0
HH	3.0	4.0	5.0	59	74	89	1.0
OHH	3.0	4.0	5.0	240	300	360	1.0

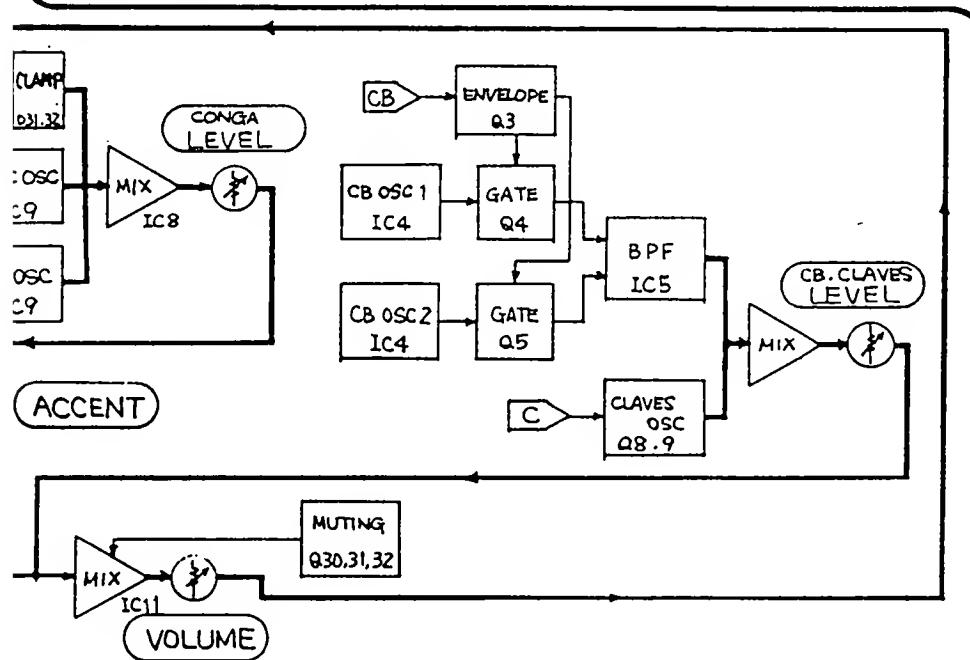




20 21 22 23 24 25 26 27 28 29 30 31 32

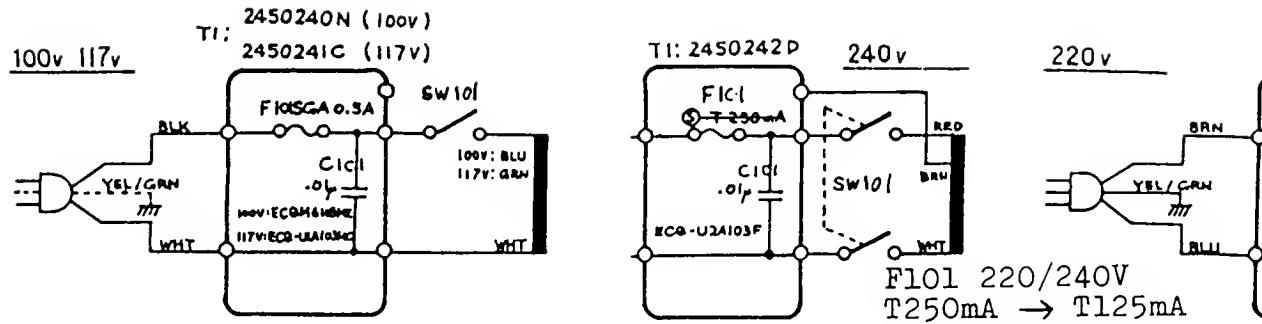


CONTROL BOARD

CR-5000  
BLOCK DIAGRAM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

A



B

C

D

E

F

G

H

I

J

K

L

M

N

O

P

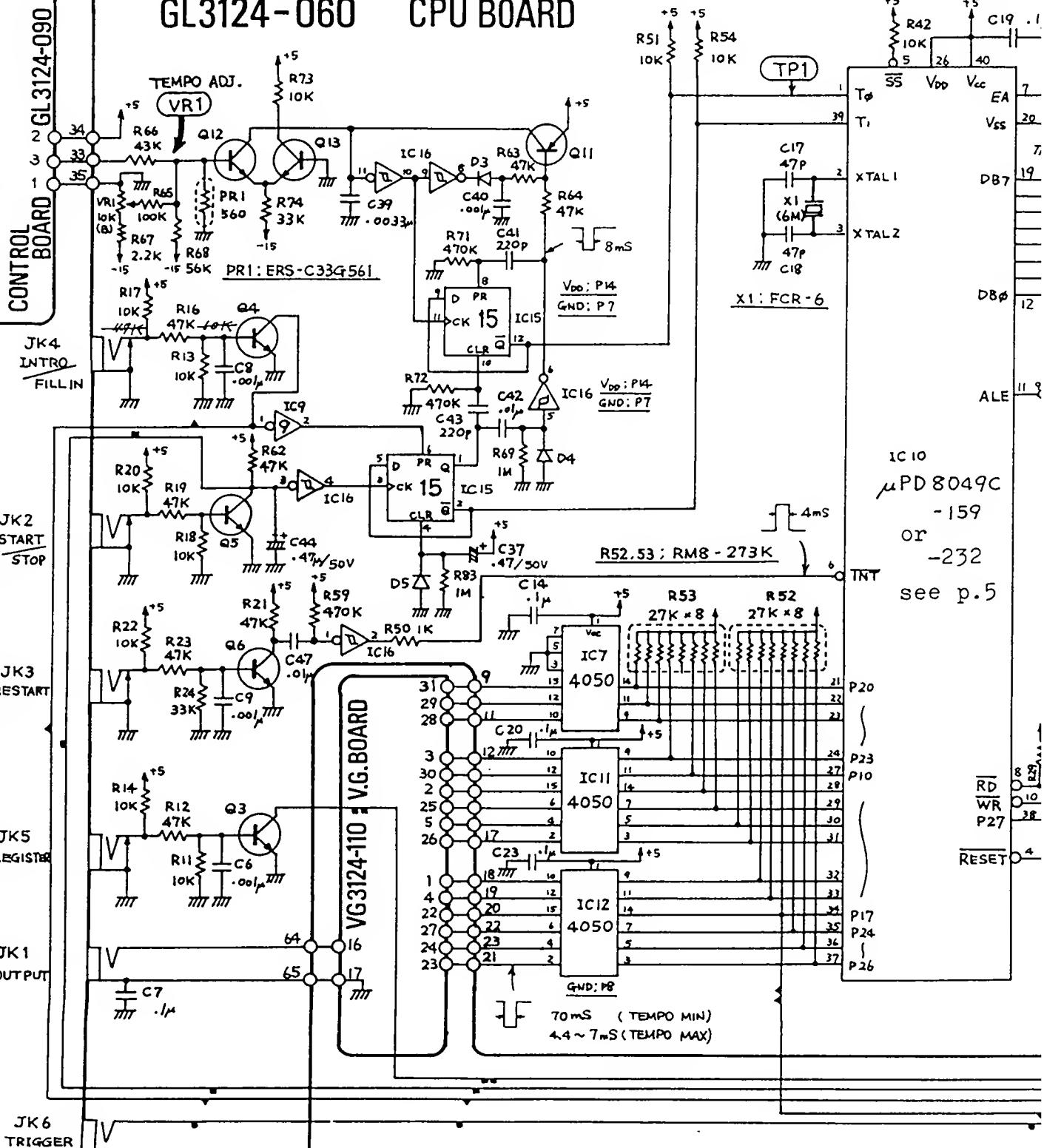
Q

R

S

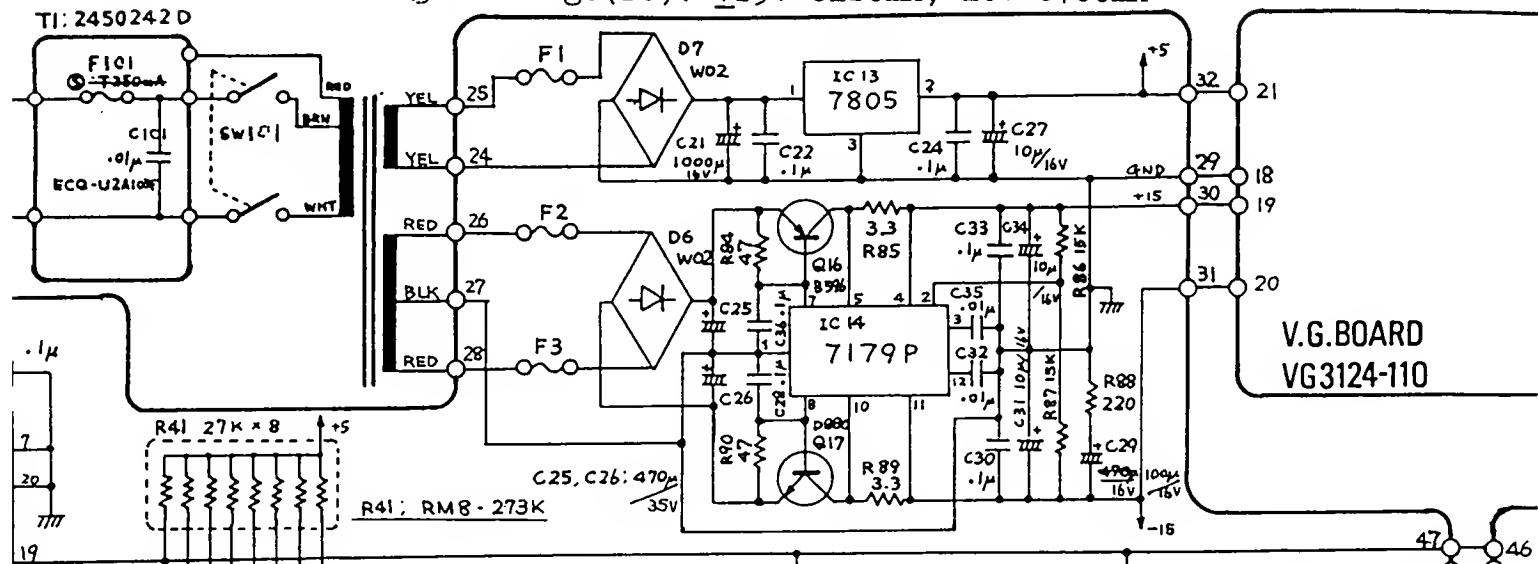
T

## GL3124-060 CPU BOARD

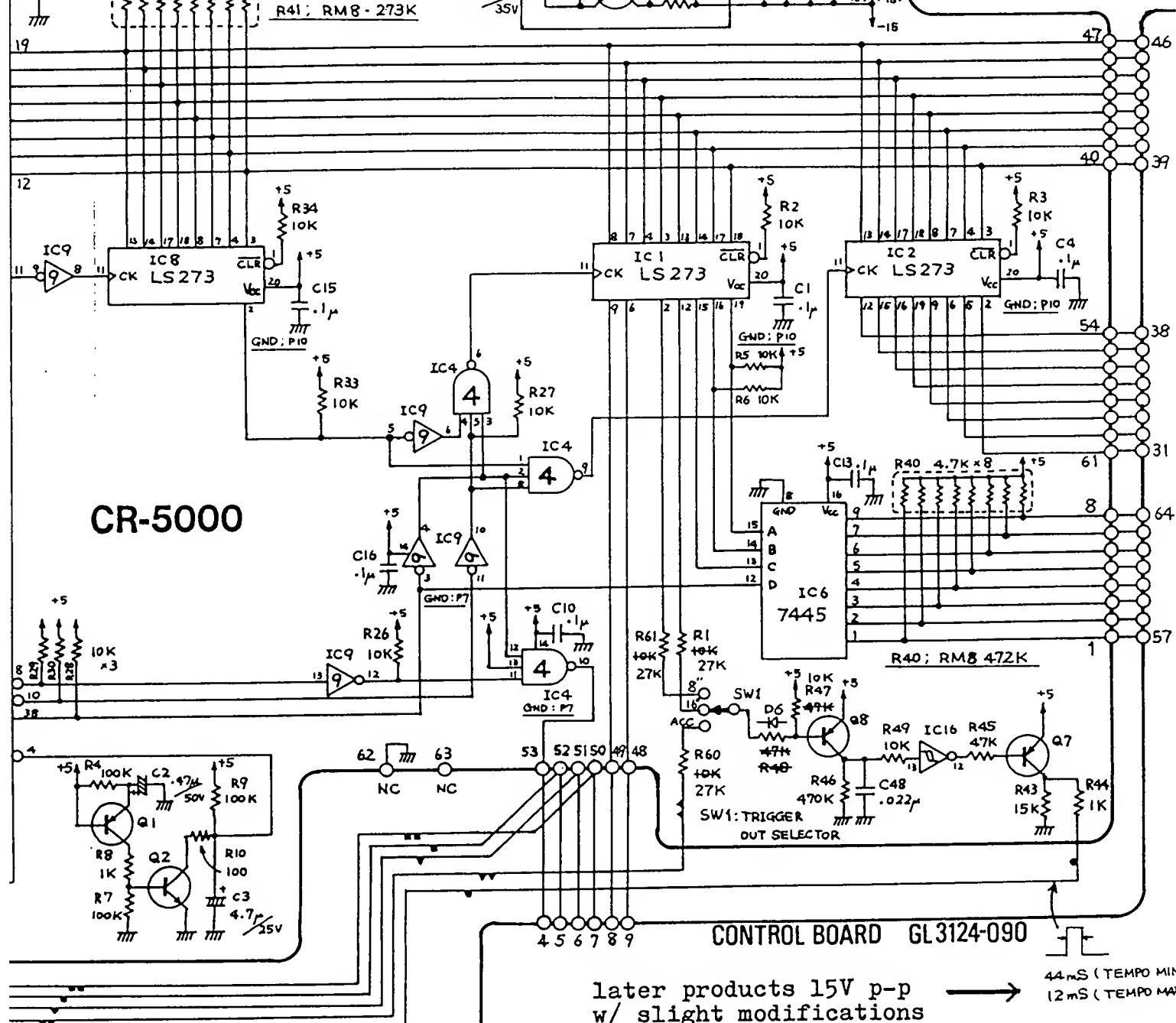


20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

Sec. Wirings Ratings(DC): +23V @120mA, 10V @700mA



V.G.BOARD  
VG3124-110

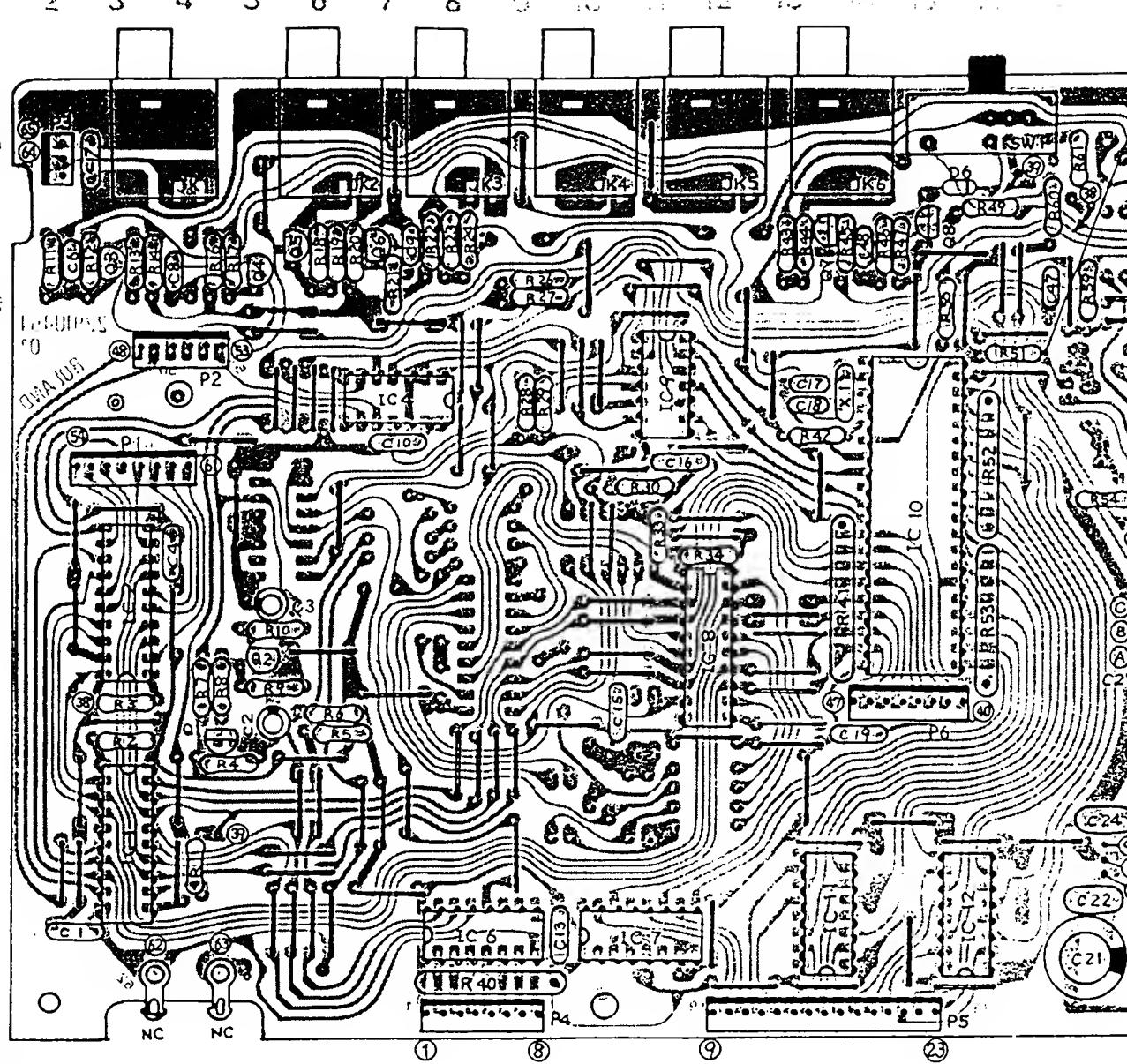


**CR-5000**

later products 15V p-p  
w/ slight modifications

44 mS (TEMPO MIN)  
12 mS (TEMPO MAX)

C.8,1981



240v

SOME MODIFICATIONS  
FOR PCB 2291046400  
AT FOIL SIDE  
SEE CR-8000 LAYOUT

	F 1	F 2	F 3
100V	jumper	jumper	jumper
117V	jumper	jumper	jumper
220V, 240V	CEE TIA	CEE T 400mA	CEE T 400mA
240V 3P	CEE TIA	CEE T 400mA	CEE T 400mA

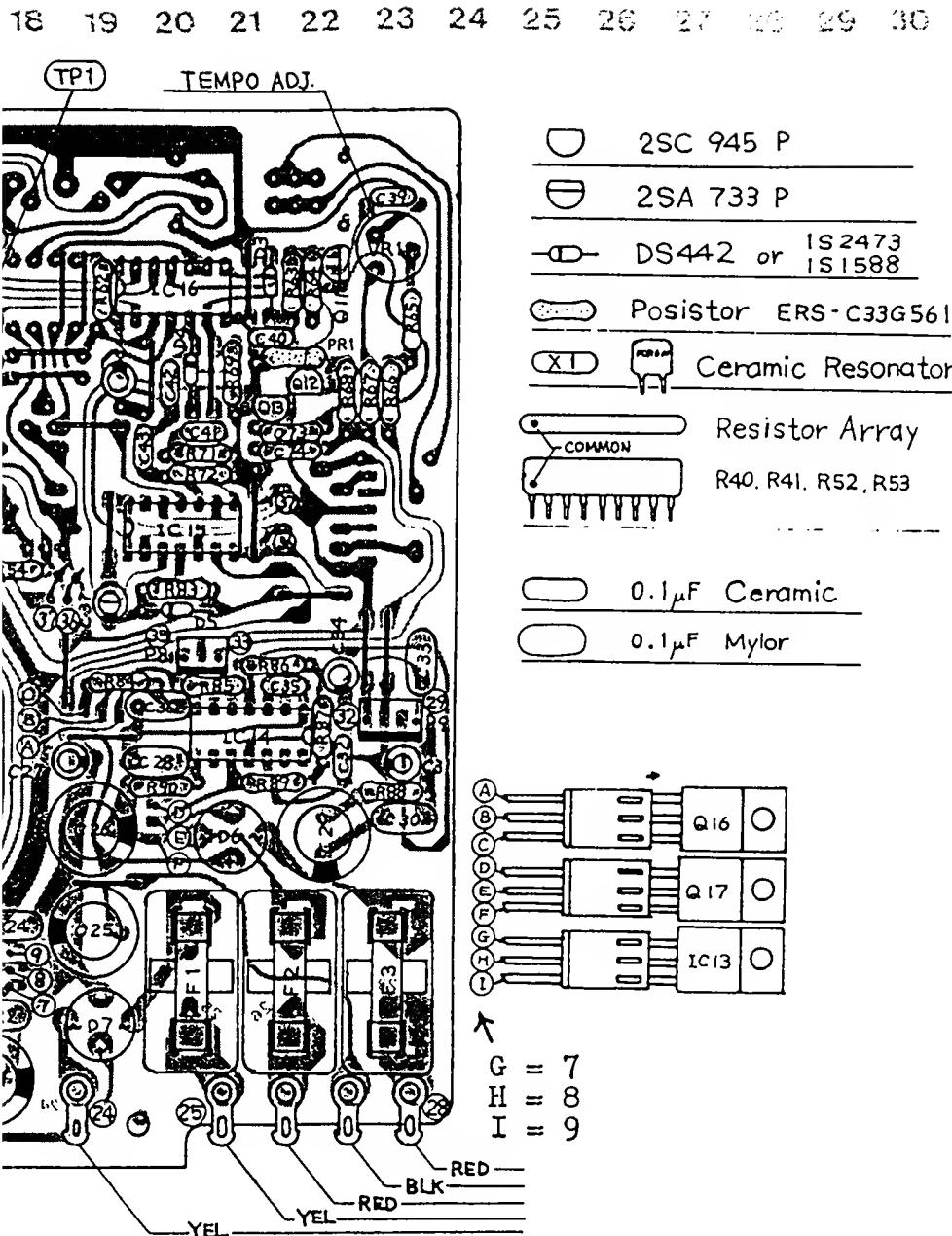
BLU—

BRN—

YEL/GRN—

IC1,2,8 : DM74LS273      IC9 : HD 74LS04P      Q1,7,8,11 ; 2SA733(P)  
IC4 : HD14023BP      D3~5 ; DS 442 or 1S2473      Q2~6,12,13 ; 2SC945(P)  
IC6 : HD7445      IC13 : 1A7805UC      Q16 : 2SB596(O)  
IC7,10,11,12 : HD14050BP      IC14 : TA7179P      Q17 : 2SD880(Y)  
IC15 : HD14013BP      IC16 : HD14584BP

HO



- 2SC 945 P
- 2SA 733 P
- DS442 or 1S2473
- 1S1588
- Posistor ERS-C33G561
- X1 Ceramic Resonator
- Resistor Array R40, R41, R52, R53
- 0.1 $\mu$ F Ceramic
- 0.1 $\mu$ F Mylar

**CR-5000  
CPU BOARD  
GL-3124-060  
(7312406008)  
(pcb 2291046401)**

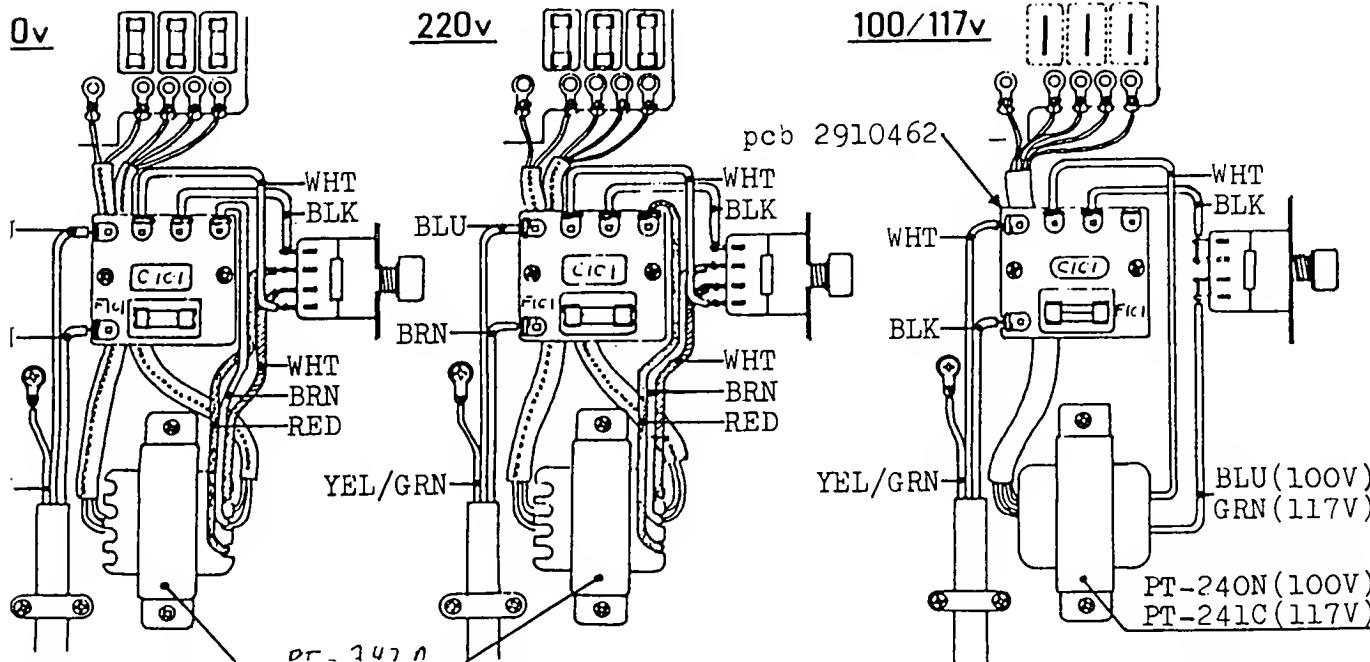
#### CHANGES IN COMPONENTS

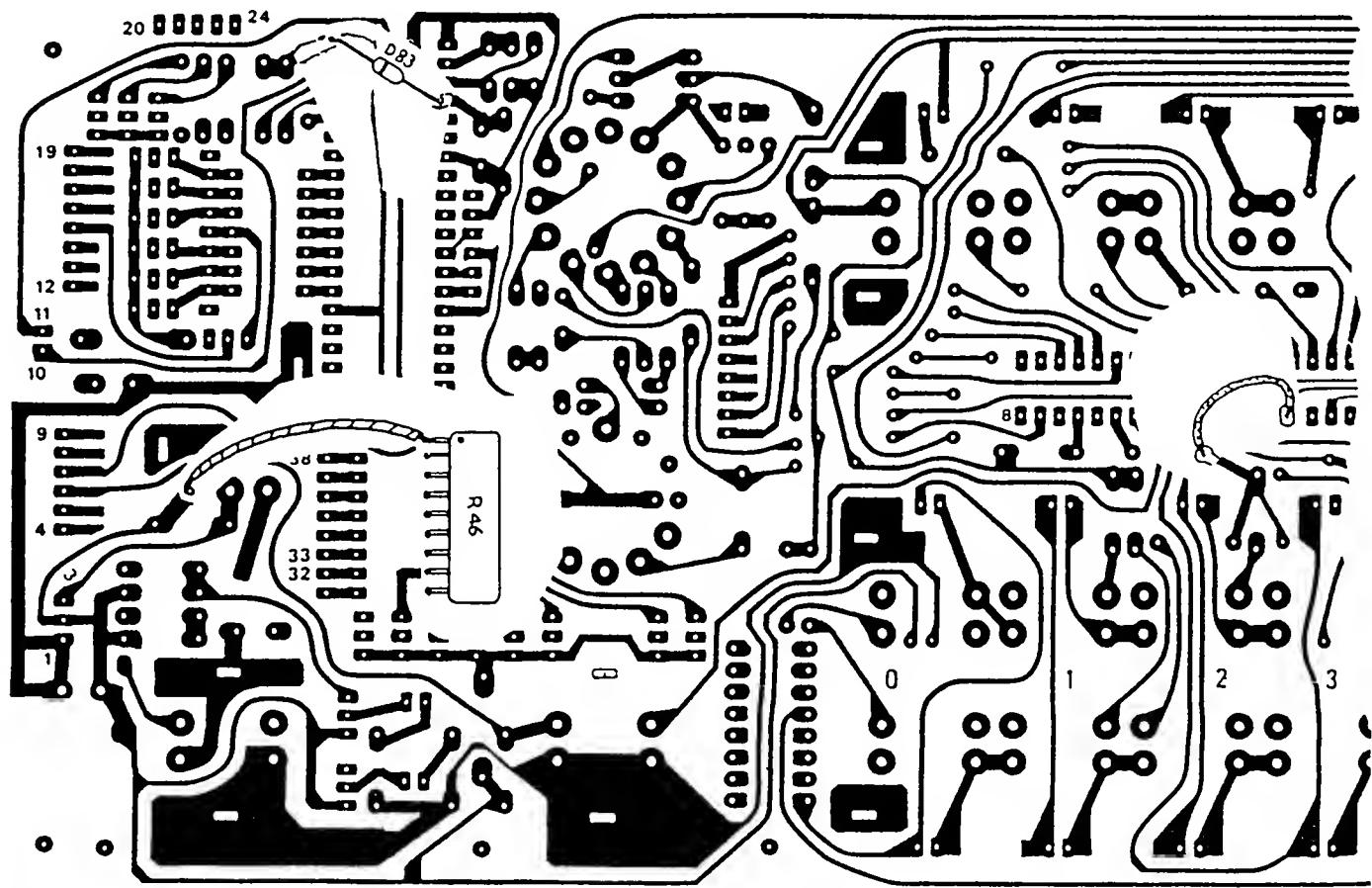
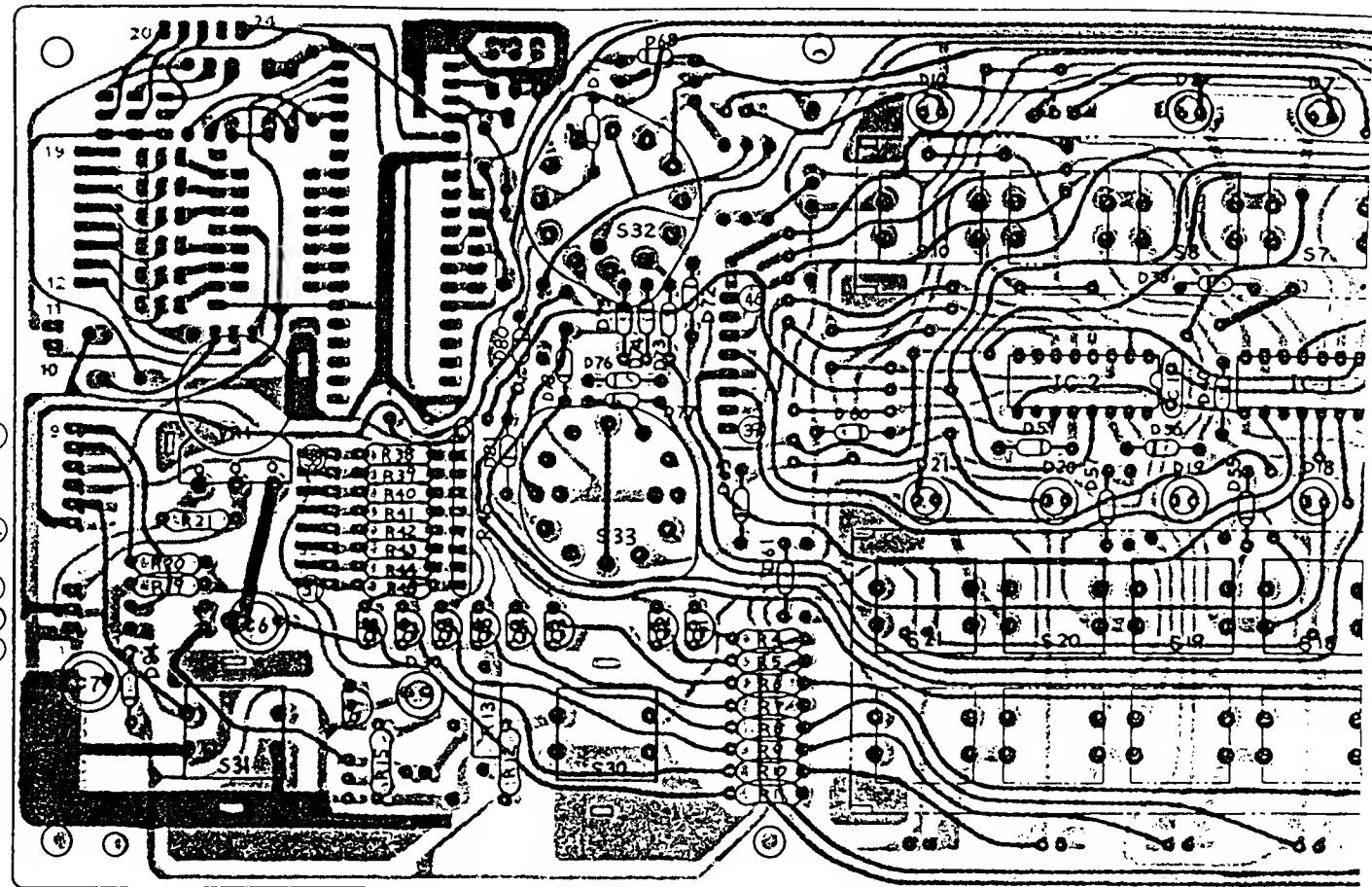
Ensure trigger outputs at IC1 when low  $V_{OH}$   
LS273 is used.

R47 47k to 10k  
R48 47k to D6  
R1 10k to 27k  
R61 10k to 27k  
R60 10k to 27k

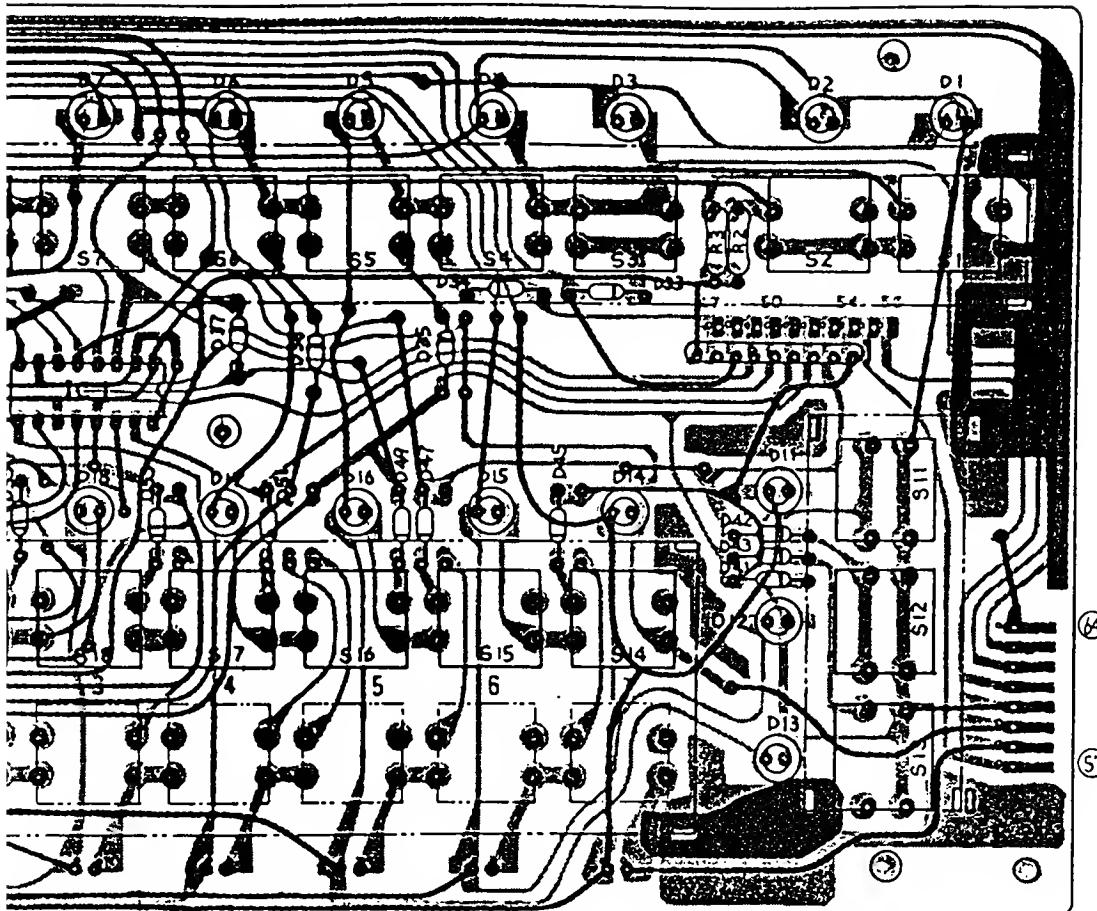
Prevents possible oscillation at final amp upon power off

C29: 470 $\mu$ F to 100 $\mu$ F





19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37



**CR-5000  
CONTROL BOARD  
GL3124-090  
(7312409010)  
(pcb 2291046501)**

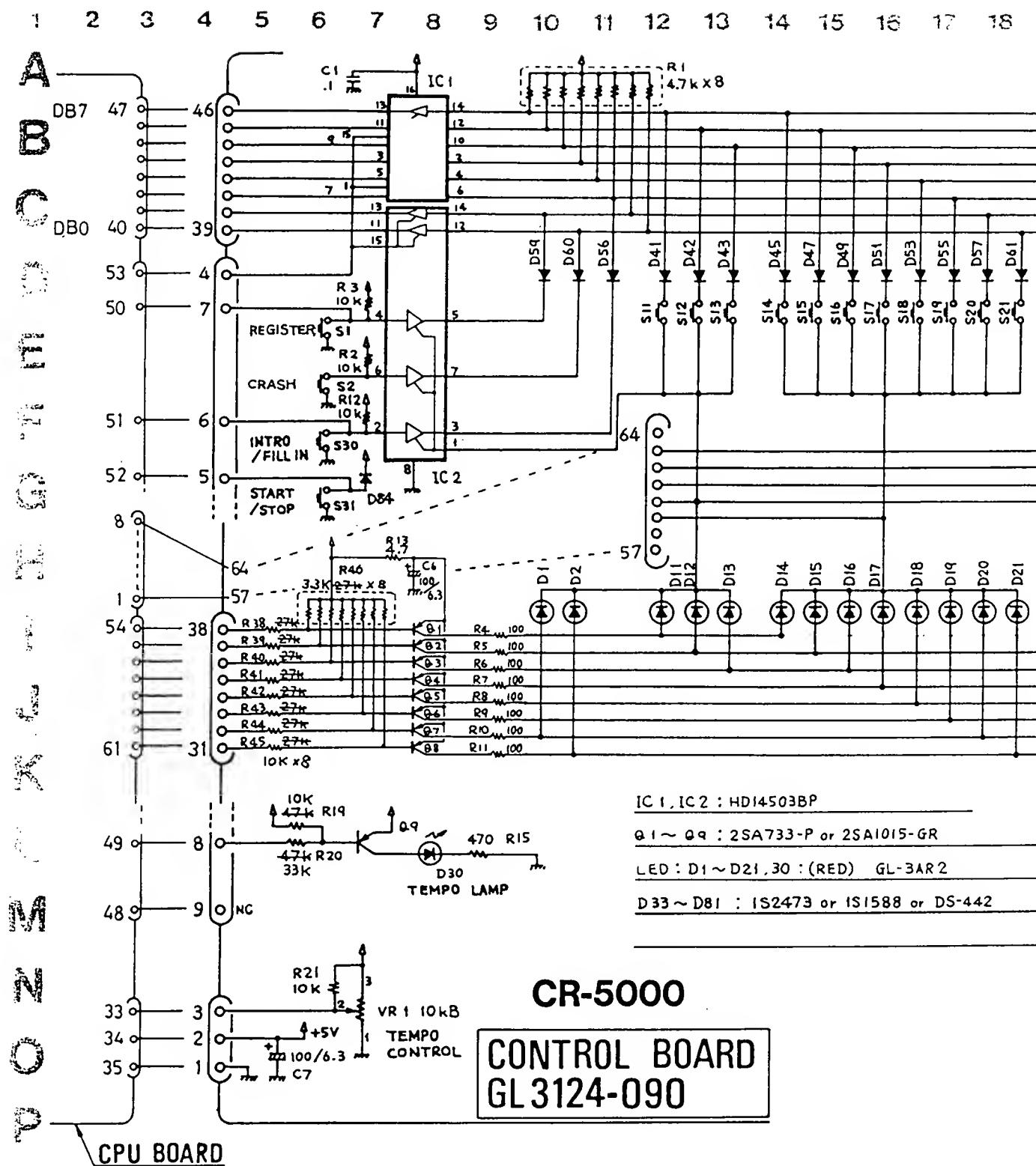
with serial number 152650

(Viewed from the rear)

-  : DS442 or 1S1588, 1S2473
-  : 2SA733P or 2SA1015-GR
-  : LED GL-3PR2 (RED)

(pcb 2291046500)

surface mounting  
D83 - CR-8000 only

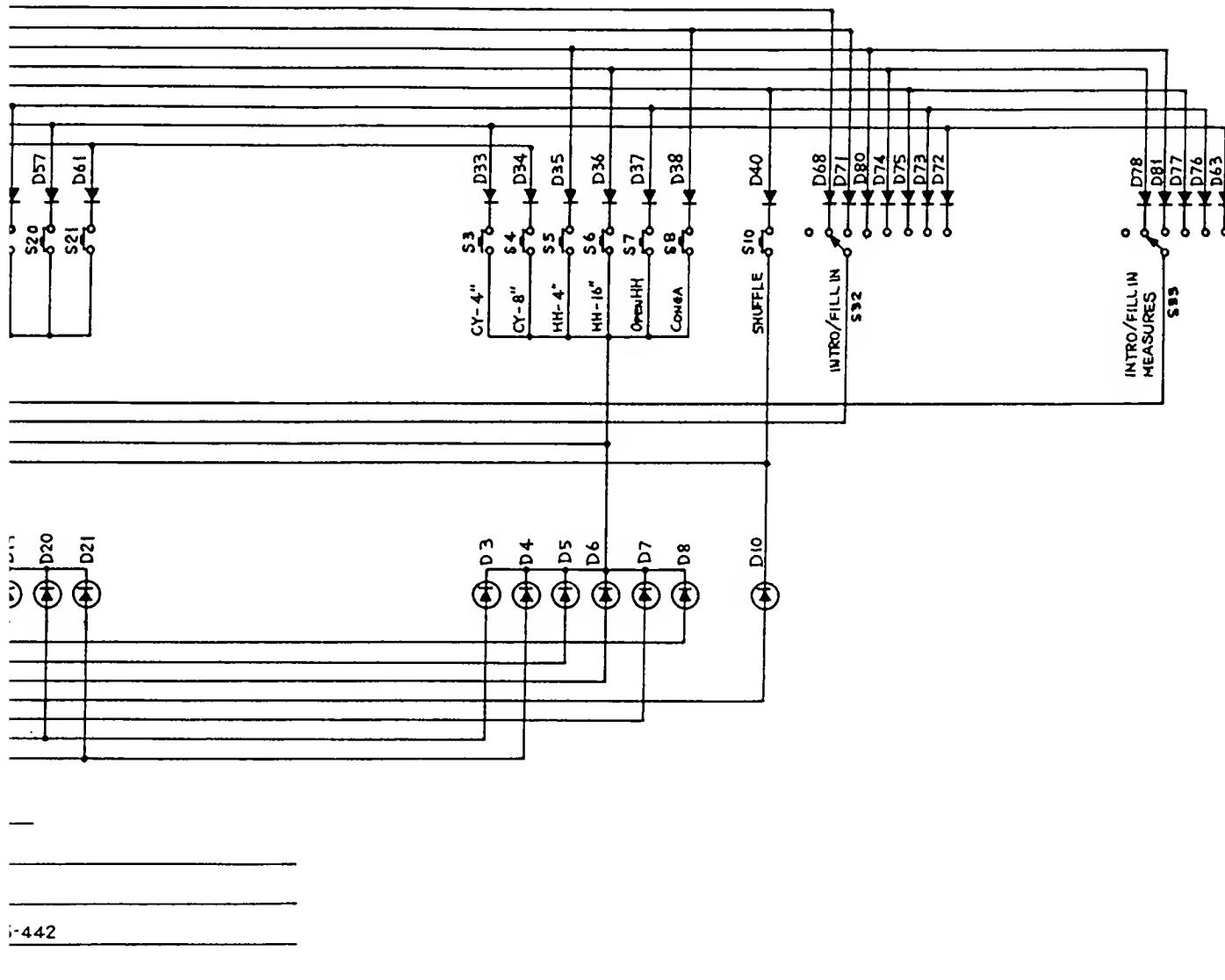


**CHANGES IN RESISTANCE With Serial Number 091100 and up**

**R** The changes eliminates possible dim lighting of LEDs due to insufficient current at IC1 or IC2 on CPU board:

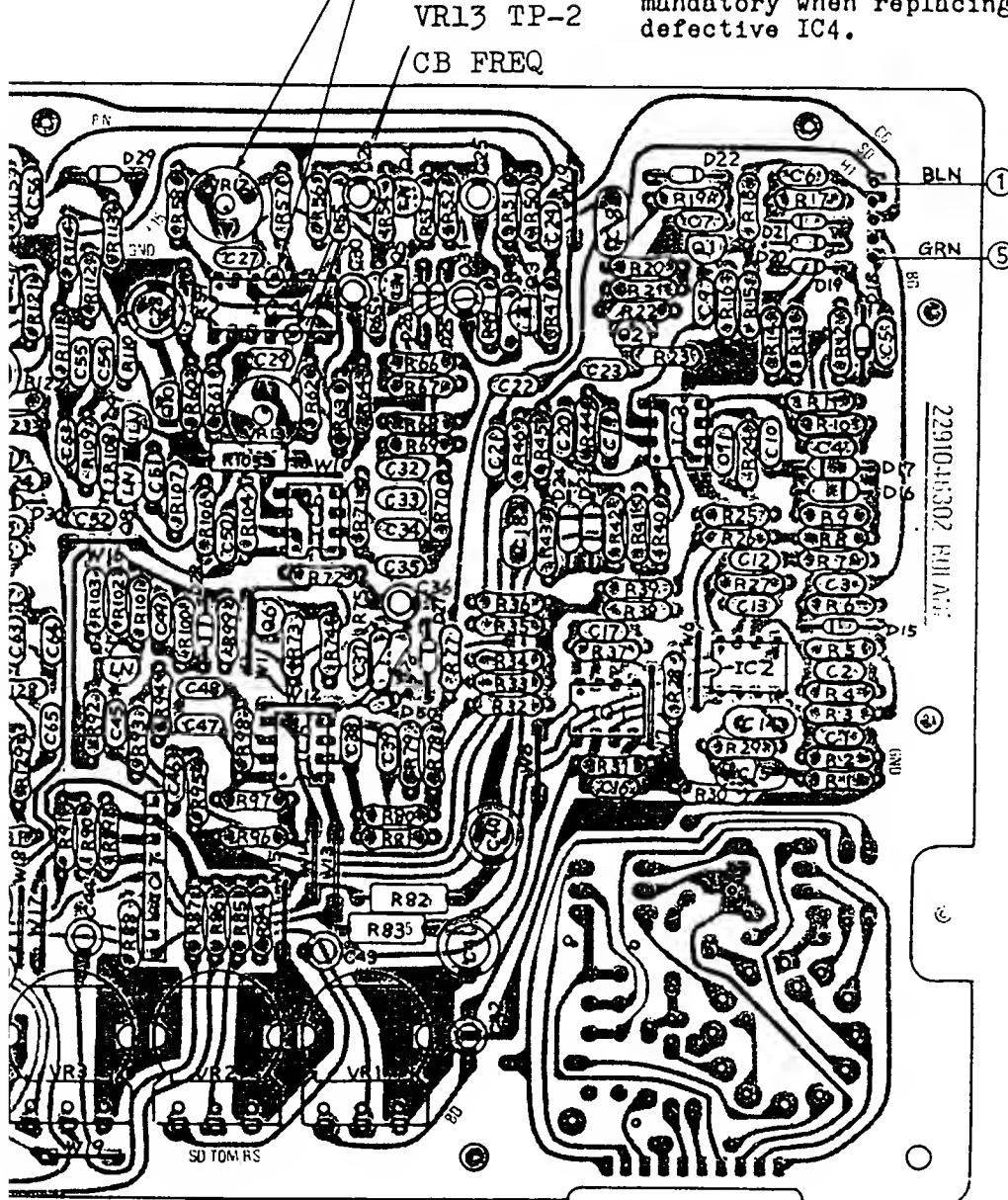
**S** R38-R45: 27k to 10k      R19: 47k to 10k      R20: 47k to 33k  
Resistor Array R46: 27k to 3.3k

18 19 20 21 22 23 24 25 26 27 28 29 30

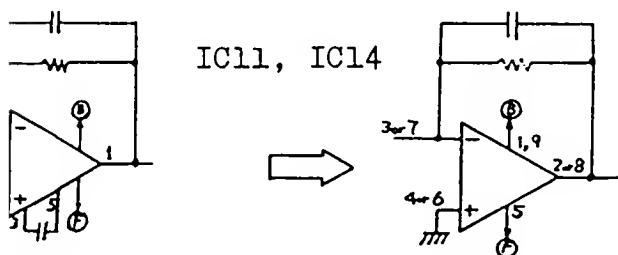


sufficient H level output



2-3  
LEVEL

VR3 VR2 VR1

57W(8-pin) or NJM4558S (9-pin)  
See p. 22 for detail.

VR12 TP-1  
CB FREQ  
VR13 TP-2  
CB FREQ

WITH S/N 111700  
R55,56,58,61,63,64  
Resistances are increased  
to limit currents into  
IC4. This modification is  
mandatory when replacing  
defective IC4.

## CHANGES IN COMPONENT WITH SERIAL NUMBERS:

**CR-5000 101400  
CR-8000 101300**

• SD

R94	330	→	2.2k
R97	33k	→	10k
R79	1k	→	15k
R80	33k	→	10k
R76	22k	→	47k
R99	4.7k	→	10k
R33	33k	→	15k
R32	33k	→	47k
R34	33k	→	22k
R100	2.2M	→	1M

C48, 47	.033μF	→	.015μF
C39, C38	.027μF	→	.0047μF
C49	.015μF	→	.018μF
C45	.0047μF	→	.0022μF
C46	.001μF	→	.015μF

• NOISE

VR11	5k(8)	→	10k(B)
R117	1k	→	open
C158	0	→	10μF/16

• TOM TOM

R46	6.8k	→	22k
R38	82k	→	33k
R39	68k	→	27k
R37	220k	→	82k
C18	.068μF	→	.018μF
C7	.01μF	→	.018μF

• CONGA

R133	120k	→	100k
------	------	---	------

• CB

R59	3.3k	→	3.9k
R56	18k	→	22k
R63	18k	→	22k

• OUTPUT

C114	100pF	→	47pF
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• ACC

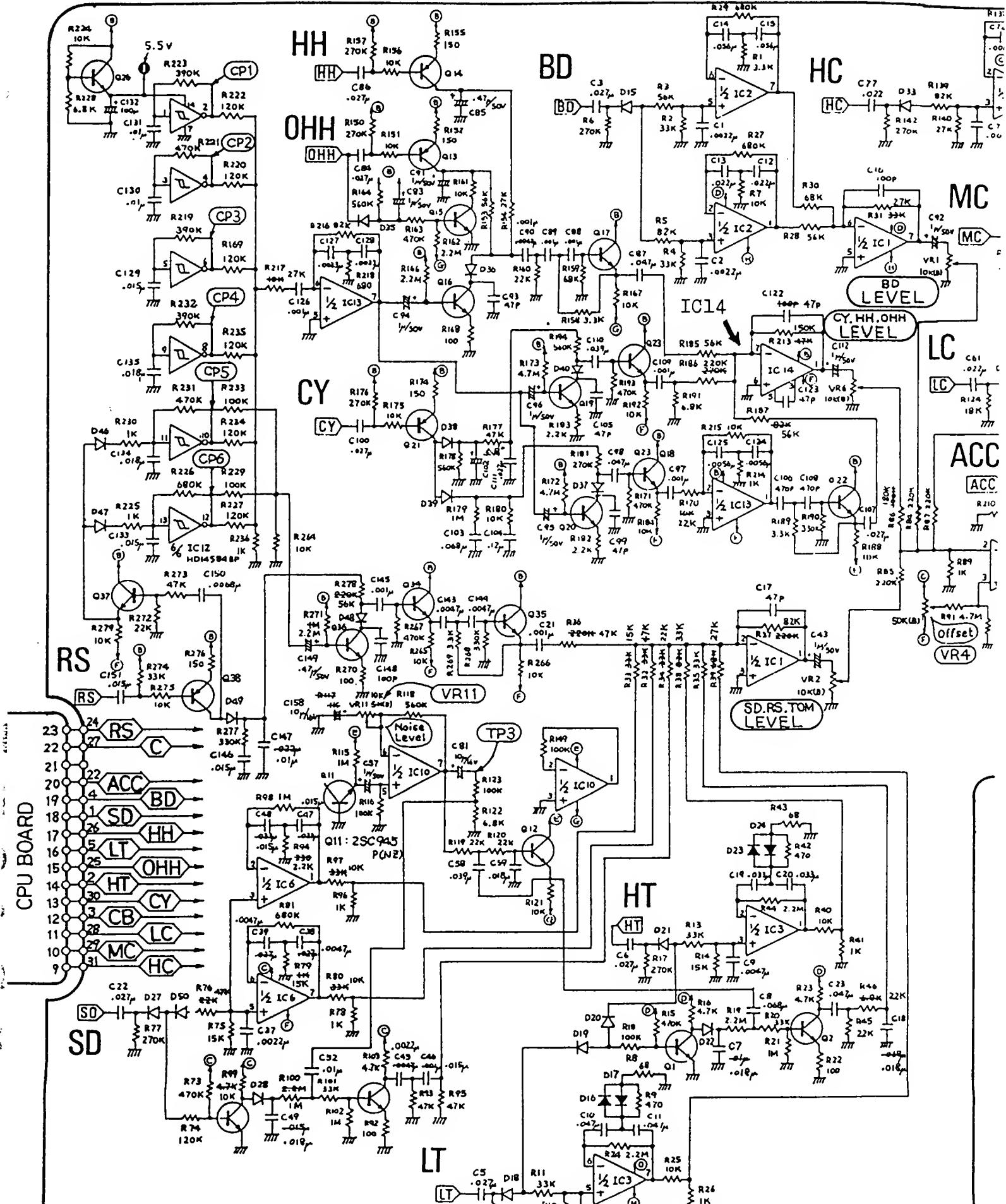
C156	0.47μF	→	1μF
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• BD

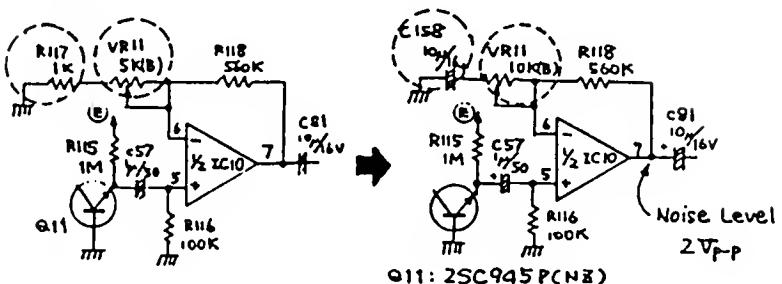
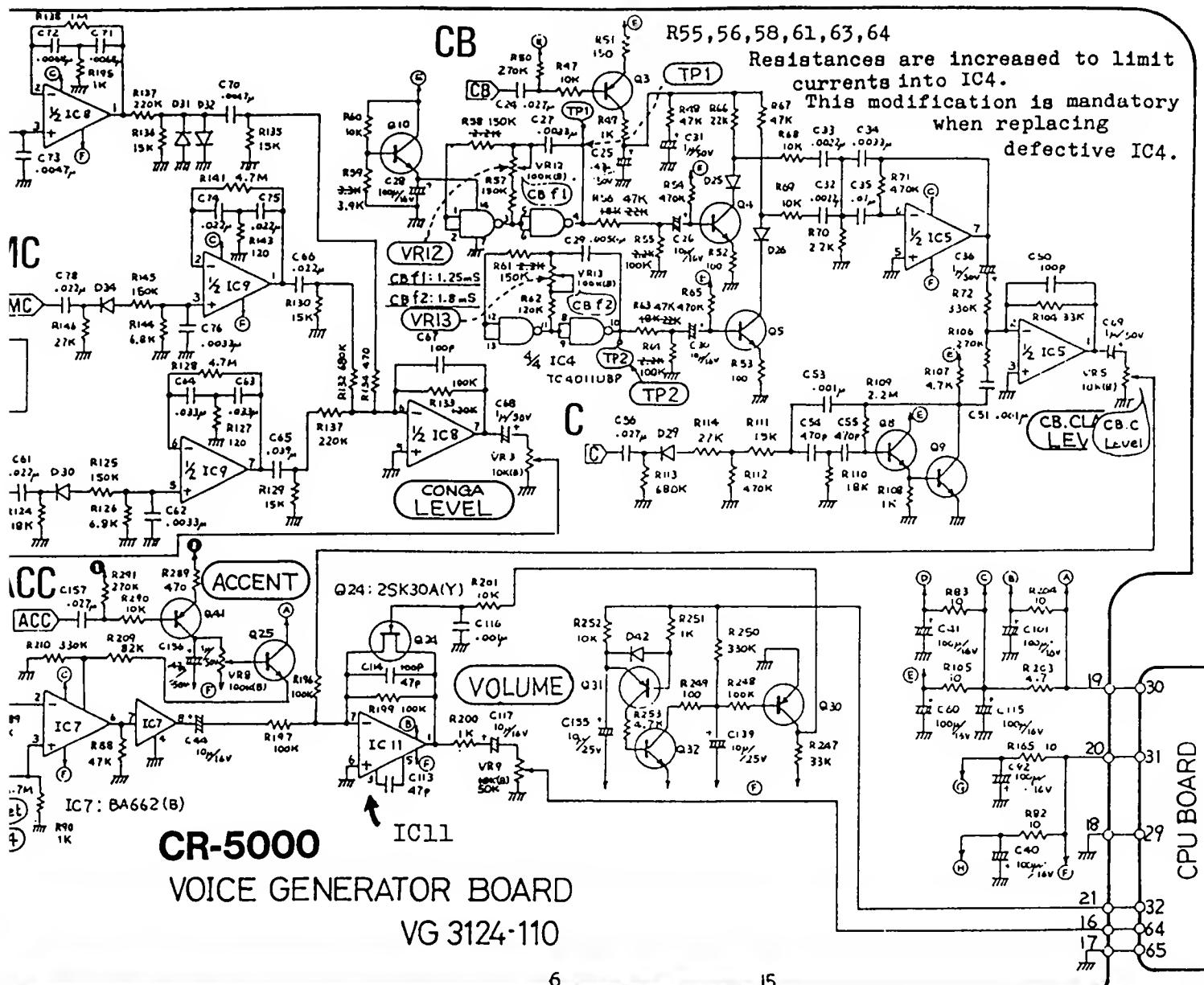
R31	3.3k	→	~
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DEC.8,1981

2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20



22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 30



IC1.2.3.5.6.8.9.10.13 : NJM4558DP

IC11.14 : HA1457W or NJM4558S

Q1.6.10.12.15.25.26.32.37 : 2SC945P

Q24.5.7.8.9.16~20.22.23.34~36 : 2SC732TM GR

Q3.13.14.21.30.31.38.41 : 2SA733P

## PARTS LIST

* CR-8000	** CR-5000	SWITCH
2201061100	Case N-611	13129117 SDKLP power 100V
*2281028102	Chassis(bottom plate) N-281	13129118 SDKLP w/CSA UL 117V
*22020159	Battery cover	13129110 ESB-70294 220/240V
*12199525	Battery holder	13159316 HSW-0372-01-030 slide TRIG OUT select. SYNC IN/OUT
*2219024802	Holder	13129714 KEH10903 RHYTHM SELECT
*2226031000	Cushion	13119508 SRM1026K15 FILL IN MEASURE
**2281027302	Chassis(bottom plate) N-273	*13119806 SRM101CY15 FILIN SELT.INSTMNT
2235010100	Rubber foot	*13159304 SSB02335 PROGRAM MODE
2281027201	Chassis N-272 power trans.	**13119704 SRM1018K15 FILL IN SELECT
*2221027100	Panel(upper) N-271	
**2221025900	Panel(upper) N-259	
*2221027200	Panel(lower) N-272	*7312506009 CPU (pcb 2291046401)
**2221026000	Panel(lower) N-260	**7312406008 CPU (pcb 2291046401)
*2222030200	Escutcheon(LED window)N-302	*7312509008 CONTROL (pcb 2291046500)
		**7312409010 CONTROL (pcb 2291046500)
		*7312512007 VOICING (pcb 2291046302)
		**7312411009 VOICING (pcb 2291046302)
		*7312511001 LED (pcb 2291046600)
		2291046200 FUSE
		JACK. SOCKET
		13449106 SG7622#8
		*13429607 DIN socket TCS0707-01-010
		FUSE
		12559104 SGA 0.500 100/117V
		12559505 CEE T125mA(s) 220/240V
		12559510 T400mA CEE(s) ±15V 220/240V
		12559513 CEE T1A(s) +5V 220/240V
		12199519 Fuse clip TF-758
		RESISTOR ARRAY
		13910107 RM8-332K 3.3K x 8
		13910101 RM8-472K 4.7K x 8
		13910102 RM8-273K 27K x 8
		POTENTIOMETER
13219229	EVHRR361B14 TEMPO, VOLUME on early units	
13219312	EVHLWAD25B14 Voice level	
13219238	EVHRR361B15 ACCENT	
13219245	EVHRR361B54 VOLUME not on early products	
13299106	EVTR4AA00B53 5kB trim	
13299101	EVTR4AA00B14 10kB trim	
13299107	EVTR4AA00B54 50kB trim	
13299102	EVTR4AA00B15 100kB trim	

## SEMICONDUCTORS

## IC

1517911700  $\mu$ PD8049C-159 CPU  
 or (See Page 5 for difference.)  
 1517913000  $\mu$ PD8049C-323  
 \*15179118  $\mu$ PD8048C-305 CPU display  
 15159105HO HD14013BP  
 15159126HO HD14023BP  
 15159128HO HD14050BP  
 15159303HO HD14584BP  
 15169304HO HD74LS04P  
 15169325CO DM74LS273N octal D FF  
 15169115HO HD7445 BCD-TO-DECIMAL DEC  
 \*15179305  $\mu$ PD444C RAM  
 15199110TO TA7179P  $\pm$ 15V regulator 1519  
 15199106FO  $\mu$ A7805UC +5V regulator  
 15159306HC HD14503BP  
 15159103TO TC4011UBP  
 15189103 NJM4558DP  
 \*15189113 AN6912  
 15189502 HA1457W (pin incompatible,  
 or see p. 22)  
 15189135 NJM4558S  
 15229803 BA662B VCA

## TRANSISTOR

15119105 2SA733P  
 15129108 2SC945-P  
 15129108A 2SC945-P(NZ) noise  
 15129104 2SC732TM-GR  
 \*15119121 2SA937-Q  
 \*15129121 2SC2021-R  
 15139101 2SK30ATM-Y  
 15119806 2SB596-O or Y  
 15129816 2SD880-O or Y

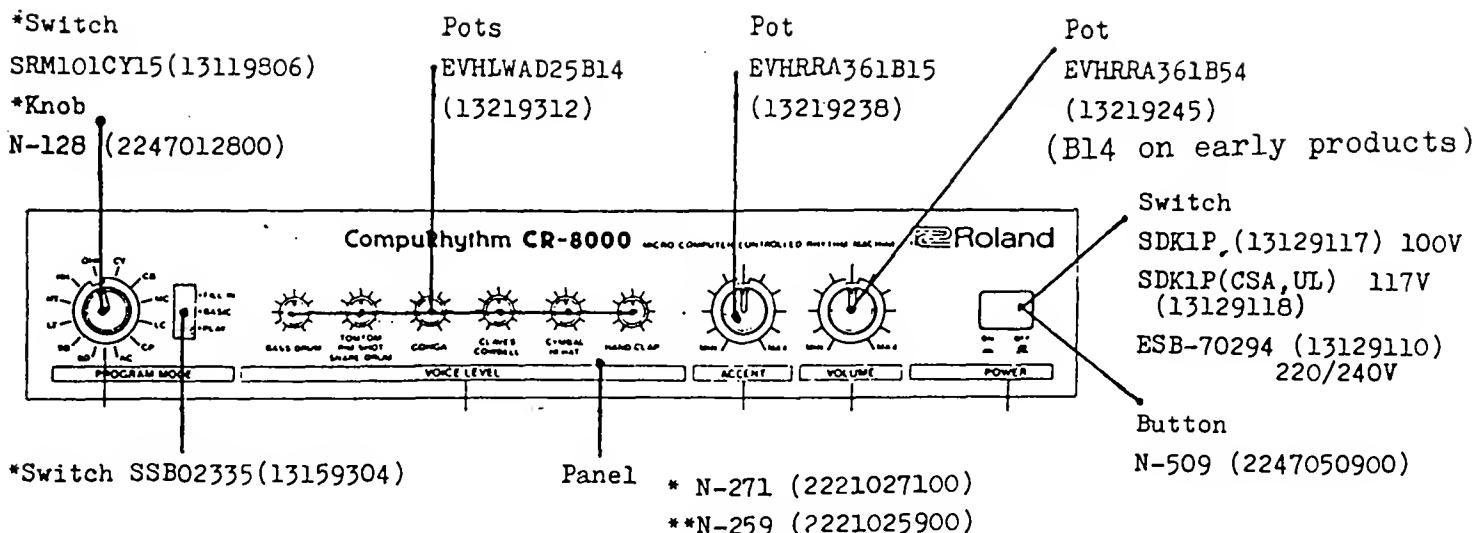
## LED

15029109 GL-3AR2 red  
 \*15029112 GL-3PG2 green BEAT  
 \*15029125 TLR312 DISPLAY

## Diode

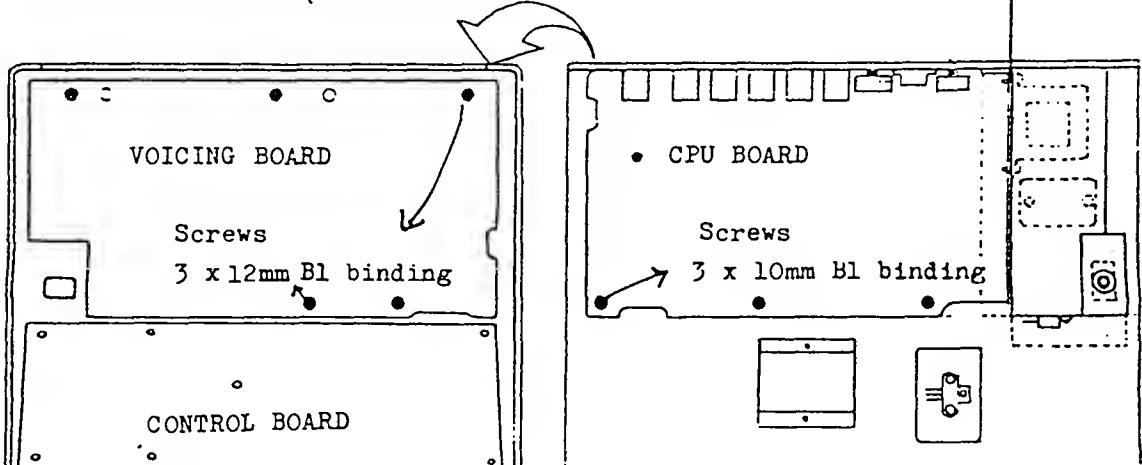
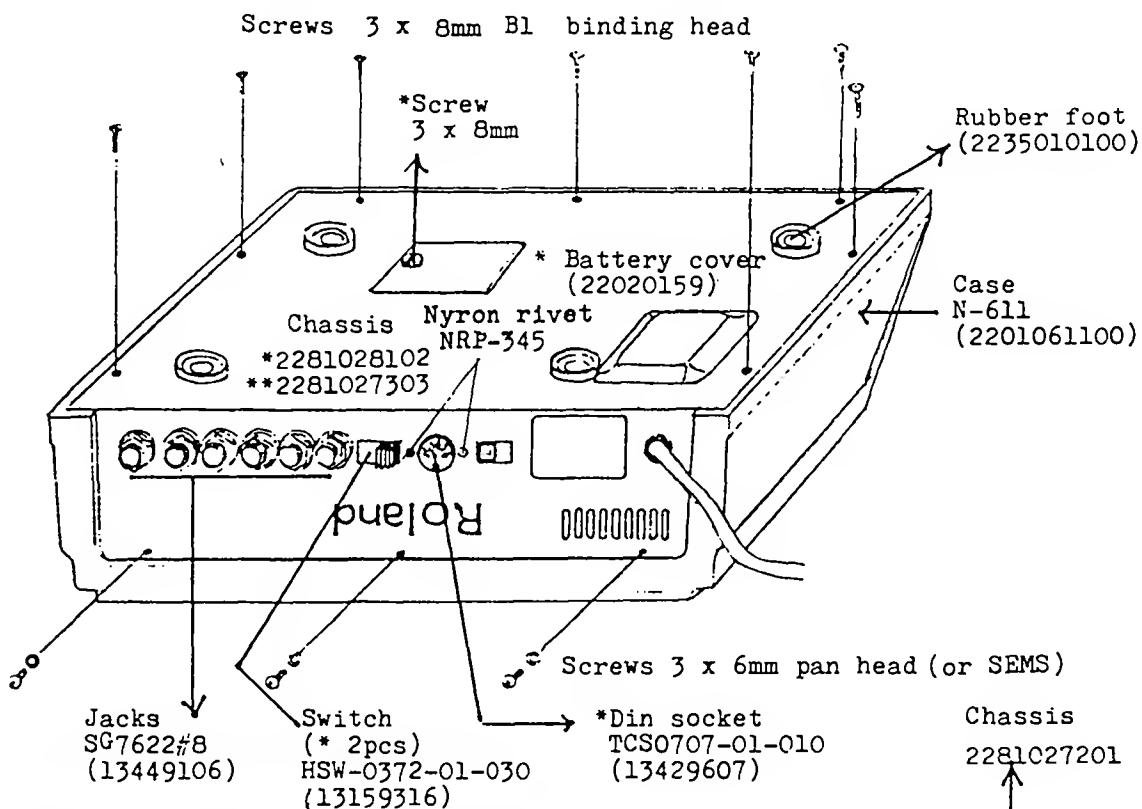
15019107 DS442 or 1S1588 or 1S2473  
 15019122 1S188FM  
 15019236 W02 bridge rectifier

12389708 FCR-6 (6.0MHz)  
 ceramic resonator



## DISASSEMBLY

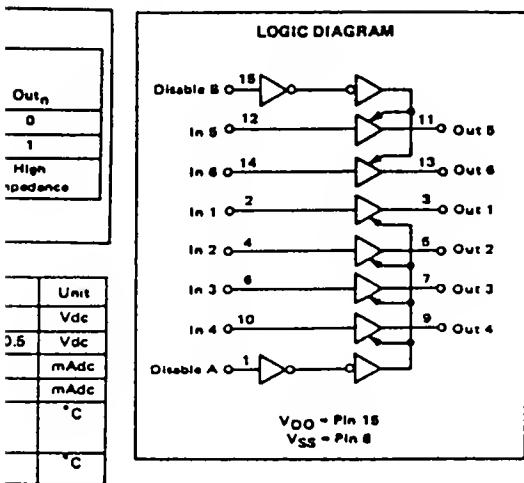
Remove ten (10) screws indicated below.





## 103B

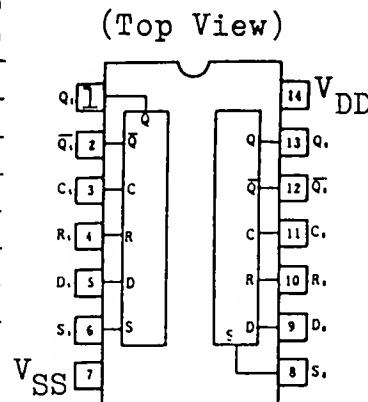
3-STATE BUFFER



## HD14013B

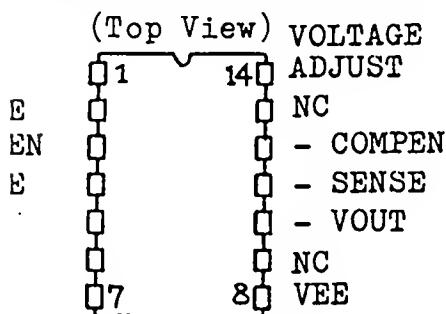
Dual Type D Flip Flop

Clock'	Data	Reset	Set	OUT	
				Q	$\bar{Q}$
/	0	0	0	0	1
/	1	0	0	1	0
/	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1



## TA7179P

## 15V TRACKING REGULATOR



g.IN = 5mV(typ) (VIN=18-30V)

g.OUT = 5mV(typ) (IOUT=0-50mA)

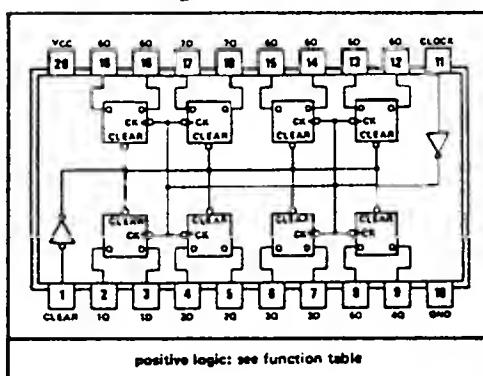
ipple rejection ratio = 75dB

tput current = 100mA (max)

## N74LS273

OCTAL D-TYPE FLIP-FLOP WITH CLEAR

(Top View)

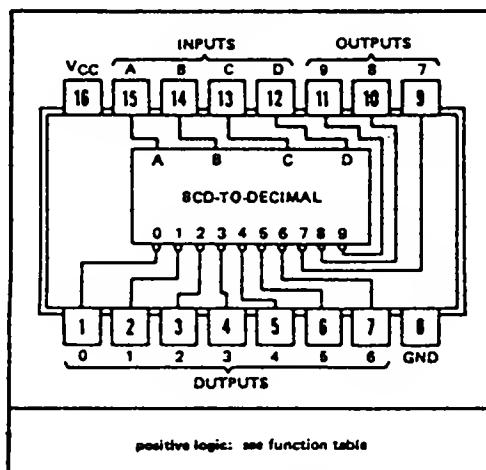


FUNCTION TABLE (EACH FLIP-FLOP)	
INPUTS	OUTPUT
CLEAR	CLOCK D
L	X
H	1
H	1
H	L
L	X

## N7445

BCD-TO-DECIMAL DECODERS/DRIVERS

(TOP VIEW)

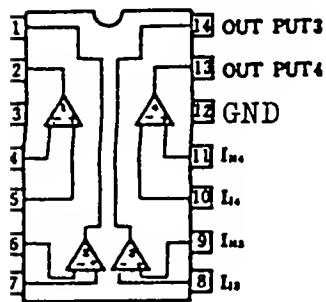


## PC177C, AN6912

Quad Comparator

## Connection Diagram

(Top View)



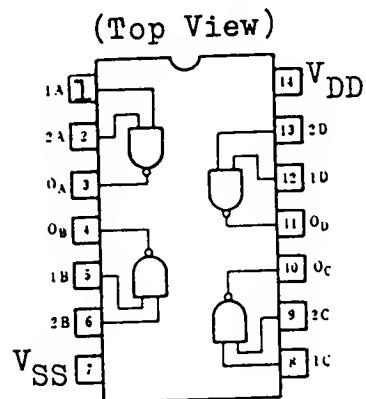
FUNCTION TABLE

NO.	INPUTS	OUTPUTS
	D C B A	0 1 2 3 4 5 6 7 8 9
0	L L L L	L H H H H H H H H
1	L L L H	H L H H H H H H H
2	L L H L	H H L H H H H H H
3	L L H H	H H H L H H H H H
4	L H L L	H H H H L H H H H
5	L H L H	H H H H H L H H H
6	L H H L	H H H H H H L H H
7	L H H H	H H H H H H H L H
8	H L L L	H H H H H H H H L
9	H L L H	H H H H H H H H H L
INVALID	H L H L	H H H H H H H H H H
INVALID	H L H H	H H H H H H H H H H
INVALID	H H L L	H H H H H H H H H H
INVALID	H H H L	H H H H H H H H H H
INVALID	H H H H	H H H H H H H H H H

H = High level (off), L = low level (on)

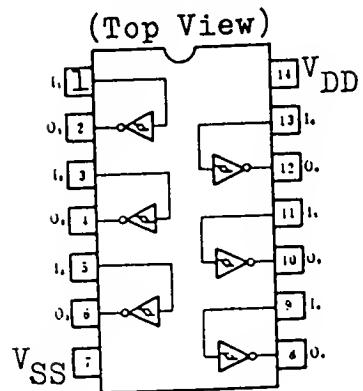
## HD14011B

Quadruple 2-input NAND Gate



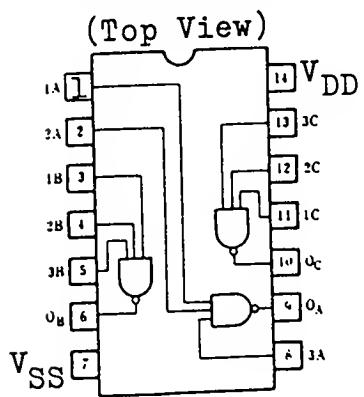
## HD14584B

Hex Schmitt Trigger

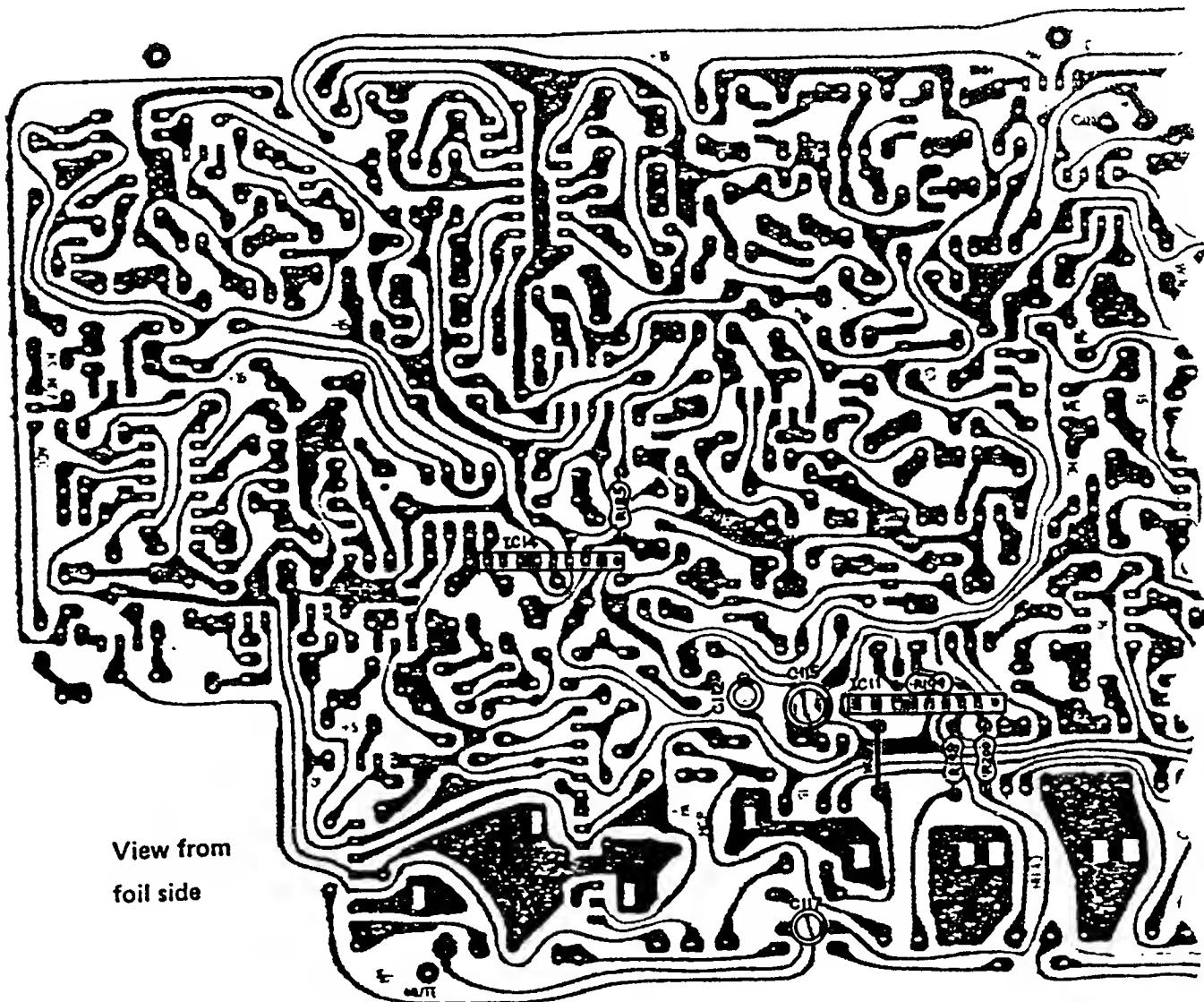


## HD14023B

Triple 3-input NAND Gate



## VOICING BOARD CHANGES



## CHANGING OPERATIONAL AMPLIFIERS

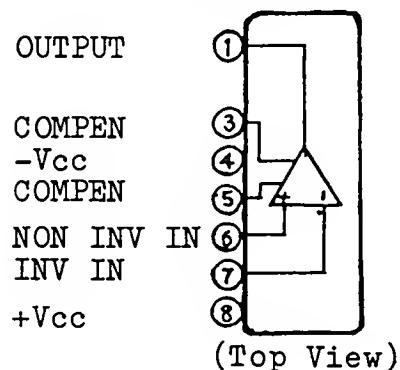
On CR-5000/8000 VG Boards as well as in other Roland products, the IC NJM4558S replaces HA1457W which is discontinued at the semiconductor manufacturer.

Incompatible pin arrangement leads to minor PCB re-layout as shown below, which is due to put into practical production.

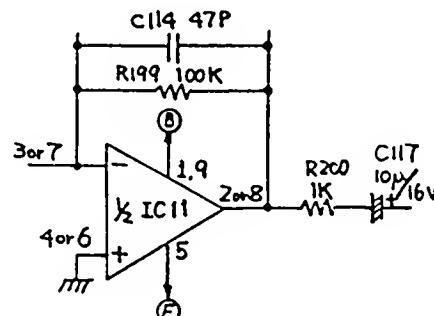
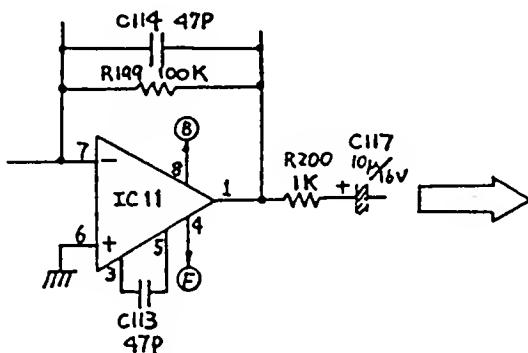
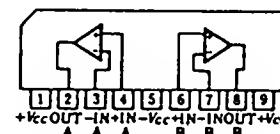
Serial Numbers with which the change is effective on the CR-5000/8000 are not fixed as of the date this edition is closed.

NOTE: Although two OP AMPS are contained in new IC, one is left redundant in this application.

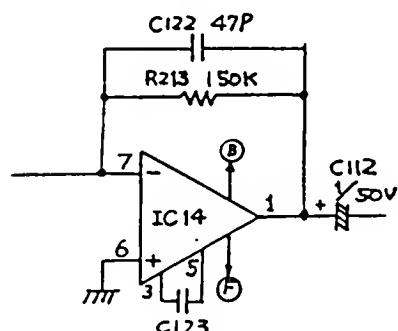
HA1457W



NJM4558S



HA1457W



NJM4558S

